



Basics on IEEE1149.x / JTAG / Boundary Scan

Introduction

Blunk electronic

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Our Services

- CAE Support and Prototyping
- Low Volume PCB assembly
- Boundary Scan Test Development
- Consulting for Design for Test (DFT)

Boundary Scan ...

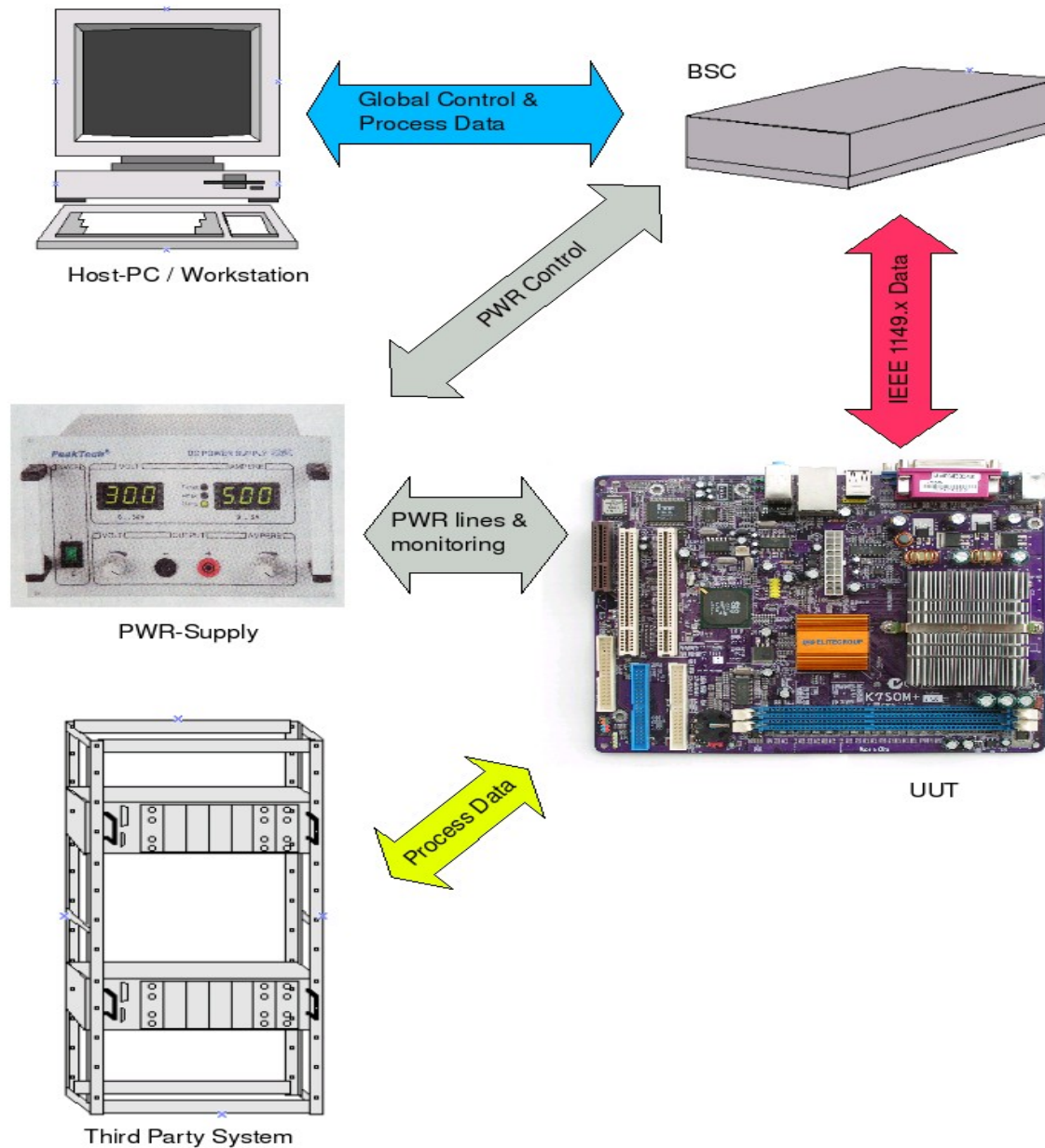
1. is a technique to test ICs, boards and systems.
2. allows access to buried nets and pins.
3. gives fault diagnostics down to pin level.
4. allows in System Programming (ISP).
5. reduces UUT access to 5 wires.
6. requires the UUT powered up.
7. bases on silicon embedded test points.
8. is standardized by IEEE 1149.x.

Why Boundary Scan ?

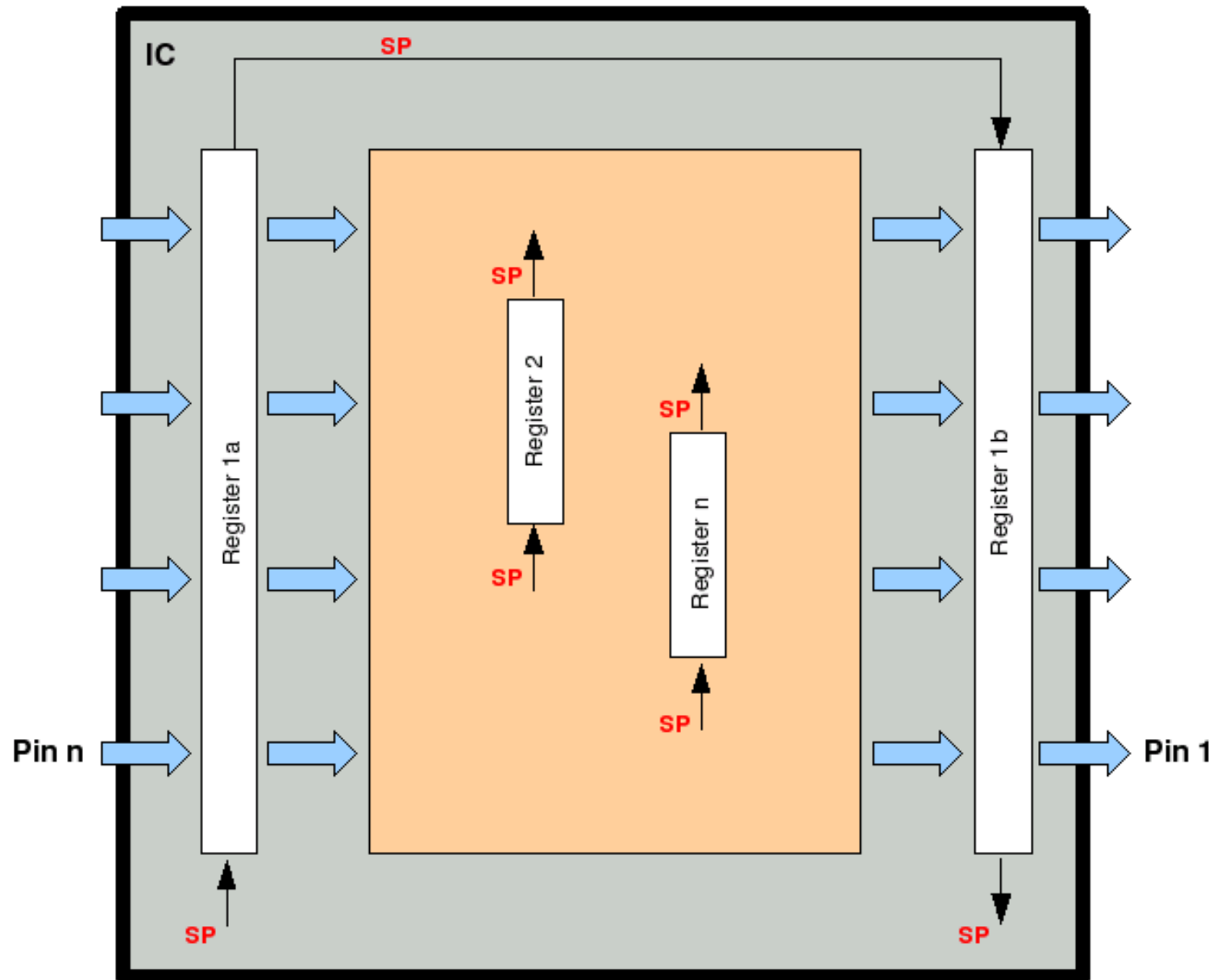
COST SAVING DUE TO:

- early design verification in design stage
- prototype test and bring up
- applicable on board and system level
- repair process simplified
- less mechanical equipment
- rapid automated test generation
- Read more at http://www.blunk-electronic.de/bsm/how_to_test.pdf

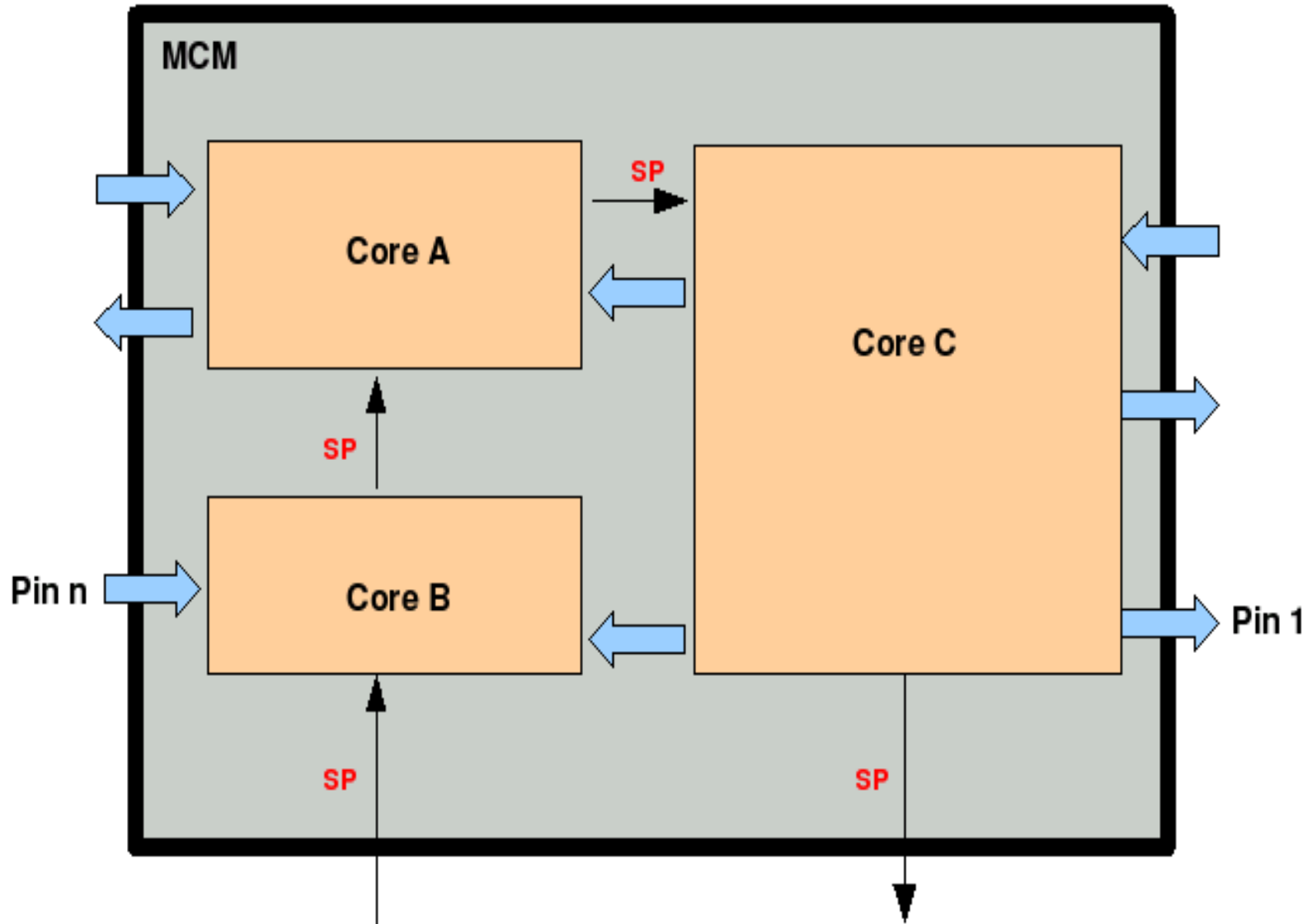
System Overview



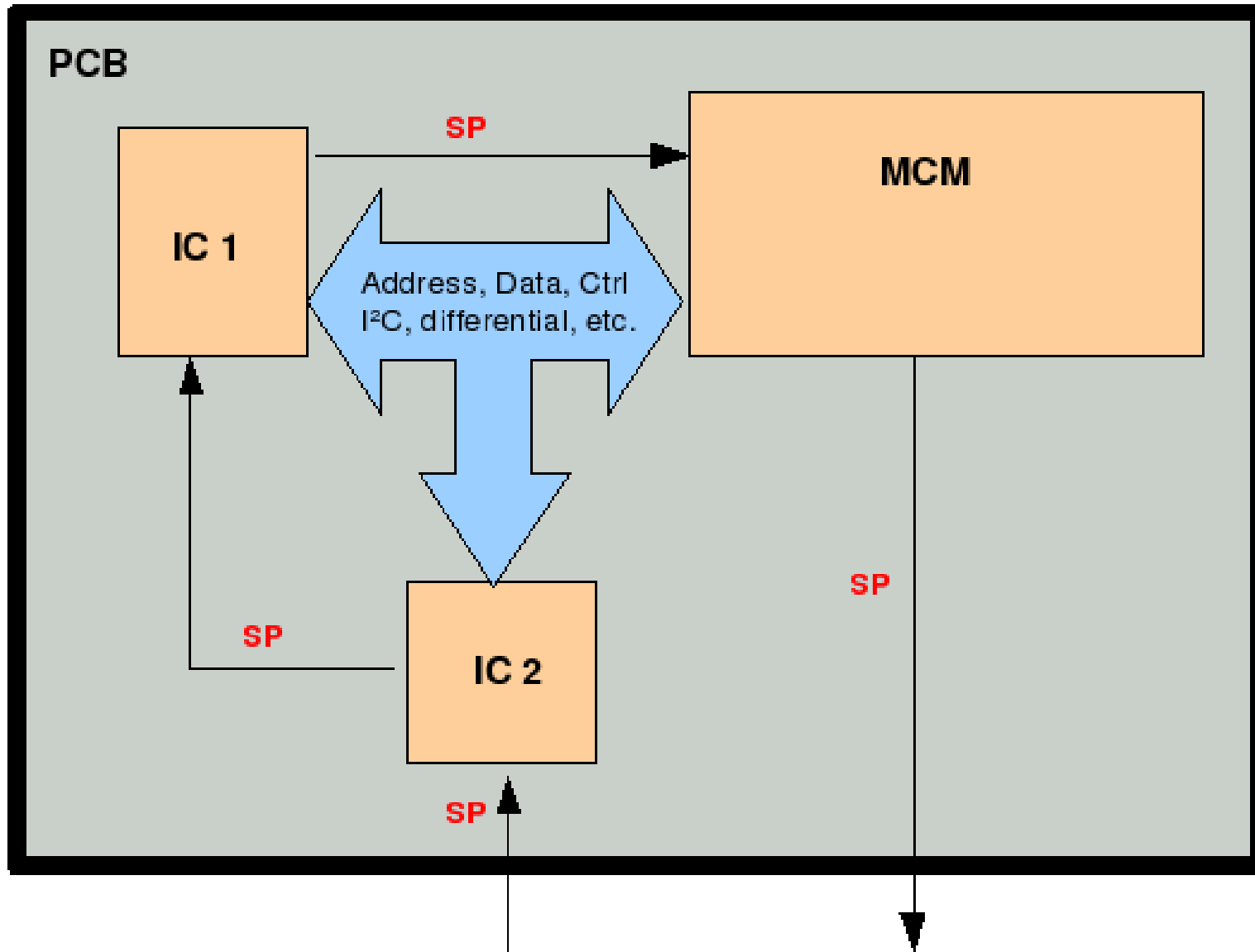
IC inside



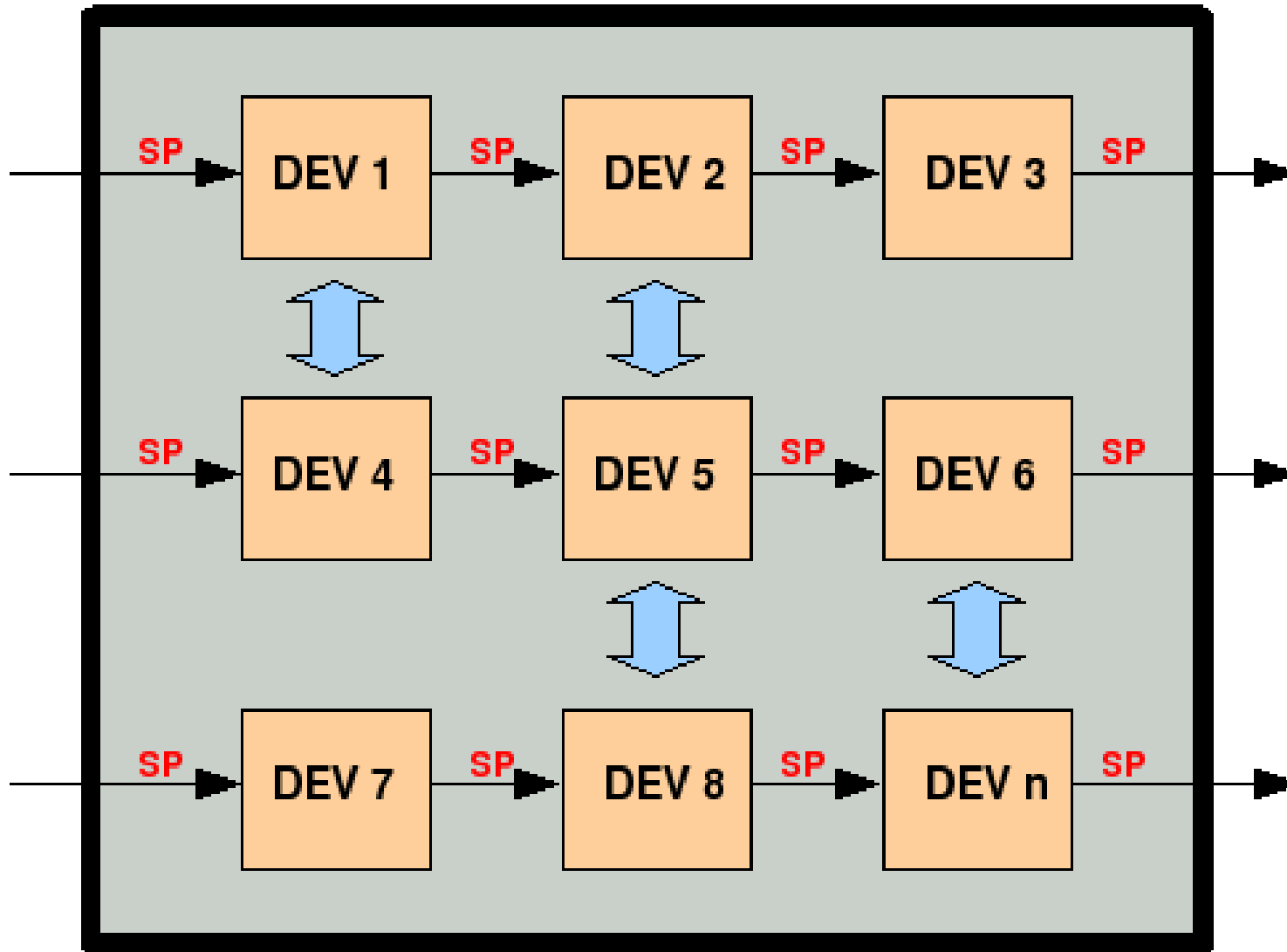
System On Chip inside



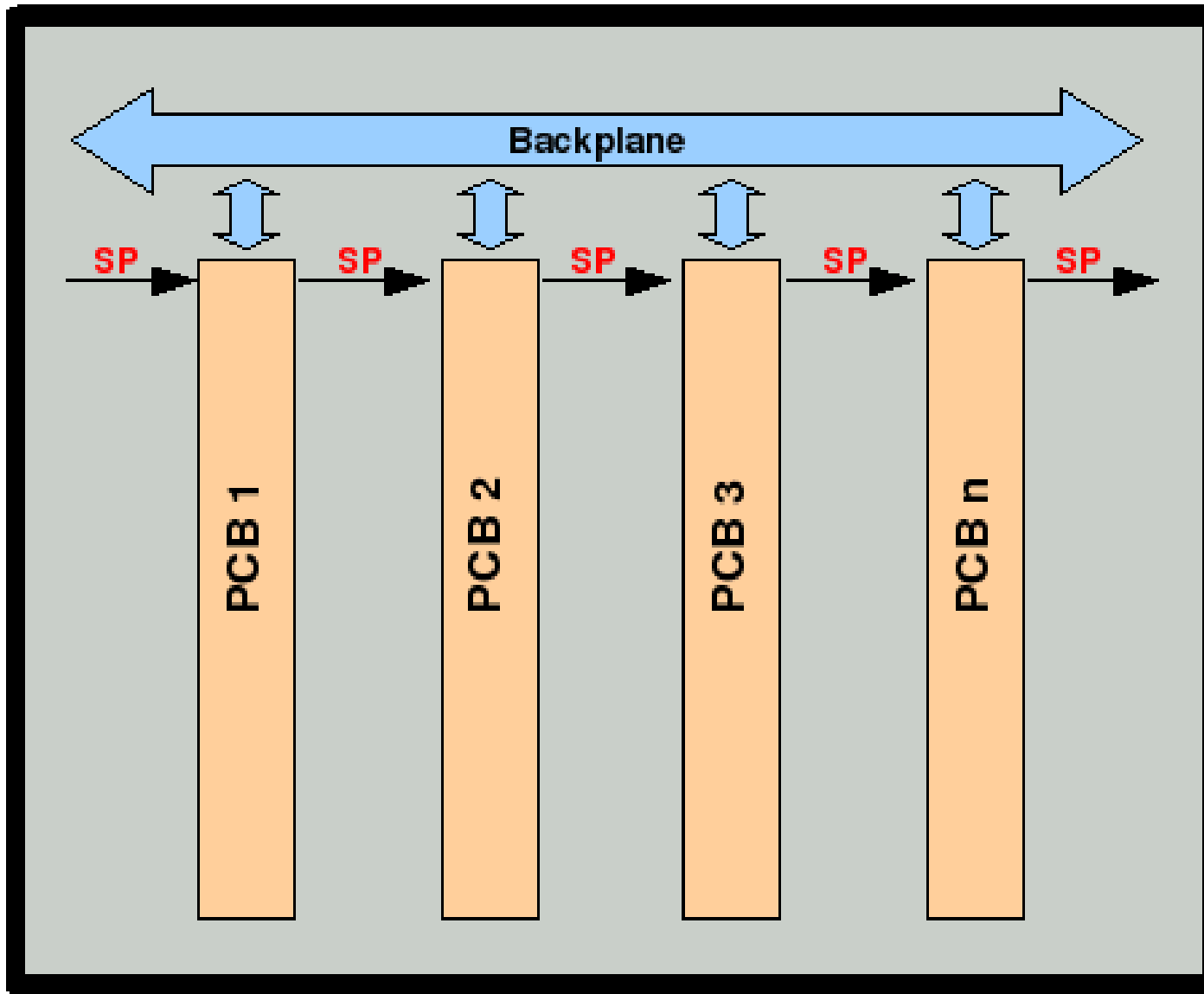
PCB Level #1



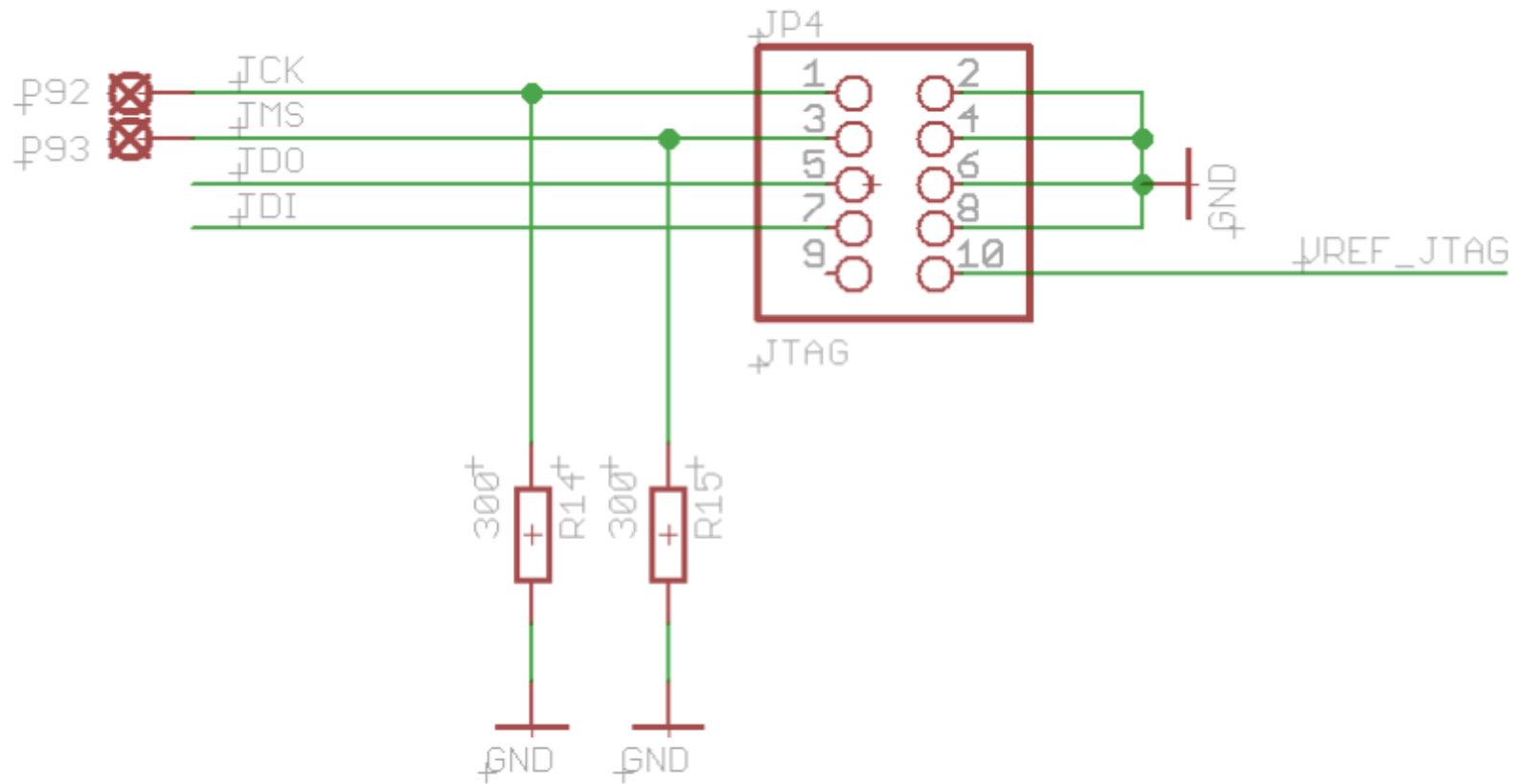
PCB Level #2



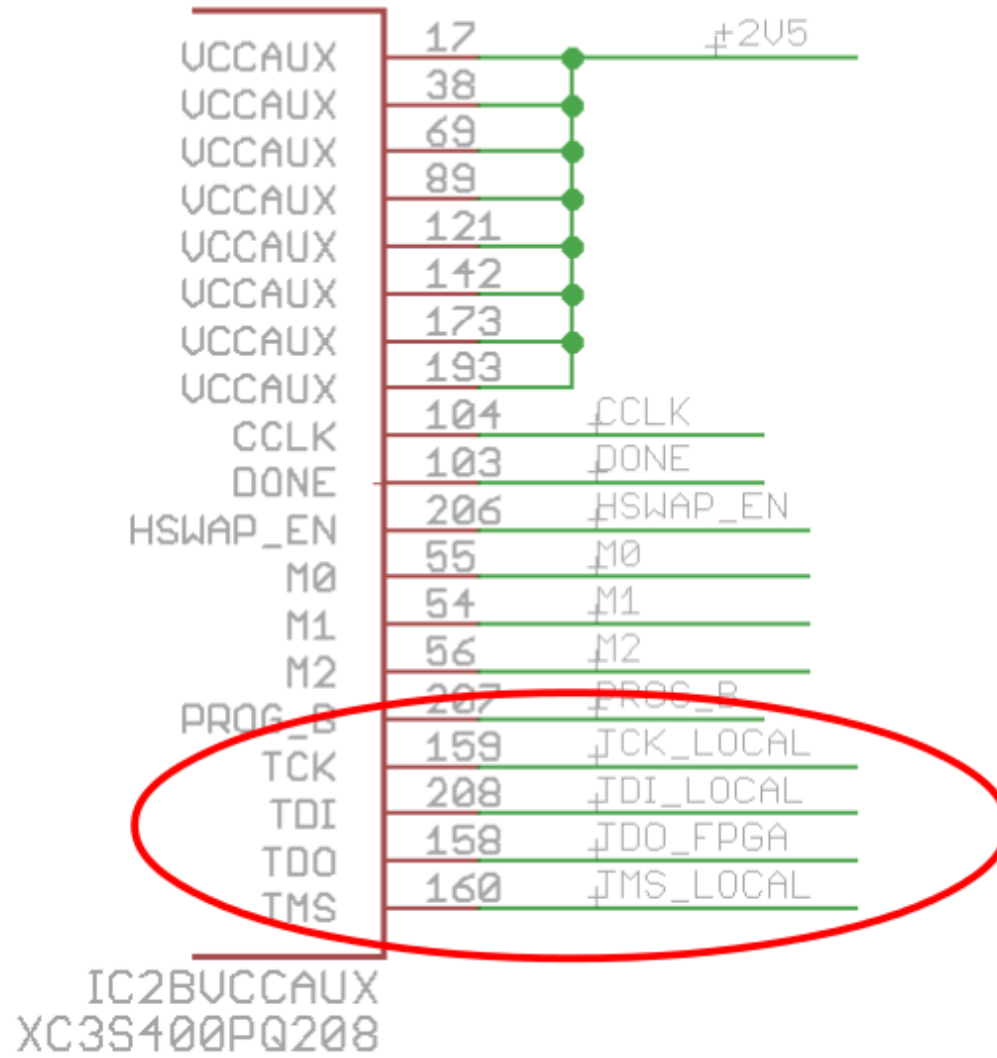
System Level



Wiring #1



Wiring #2



Links

PCB Houses in Germany:

www.q-print.de (Prototypes)

www.jlp.de (Mass Production)

Distributors and EMS in Germany:

www.technikron.de

Thanks for your attention !