Test Methods of Electronic Manufacturing

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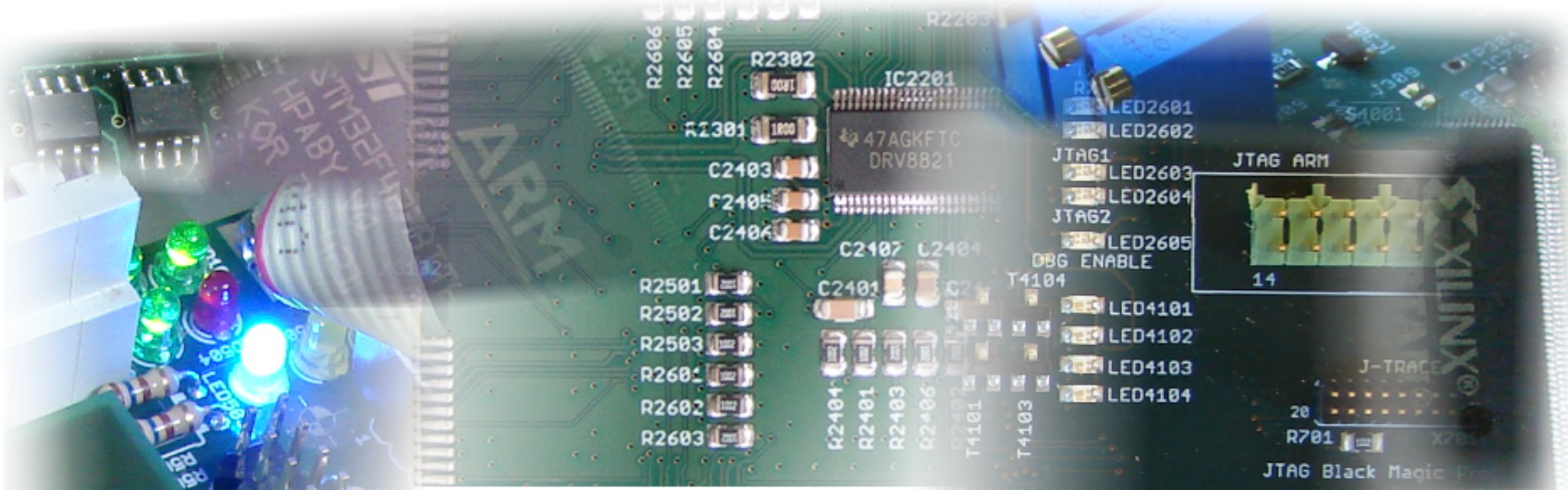
BLUNK ELECTRONIC

Design Reviews Surveys Consulting

HW/SW-Development Boundary Scan / IEEE 1149.x



Test Methods Overview

- Why testing ?
- Where do faults and defects arise ?
- What and how accurate do we test ?
- Classification of faults and defects
- Disturbances in the manufacturing process
- Place / time / costs of testing
- Criterions of test methods
- Pros & cons of test methods
- Optical tests: MVI / AOI / AXI / IRT
- In-Circuit Test (ICT)
- Flying-Probe Test (FPT)
- Boundary-Scan Test (BST)
- Self-Test (BIST)
- Function test (FT)
- Adapting
- Design for Test (DFT)

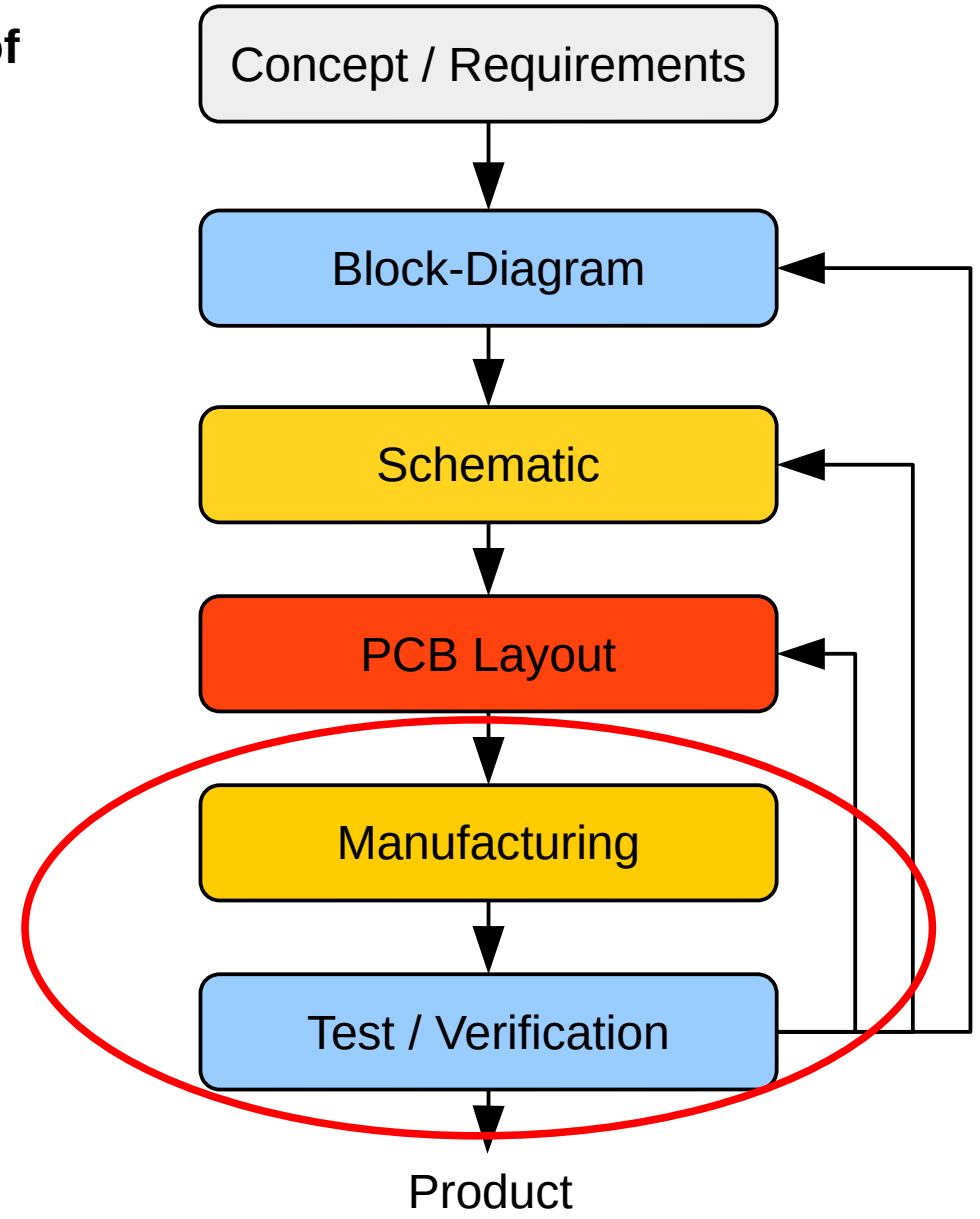
Why Testing ?

1. We want to deliver quality ! → Quality Assurance
2. Optimizung development and manufacturing
3. Save resources, engery, time, money, ...

4. Certifications (EN/IEC 61508, EN/IEC 62061, EN ISO 13849, EN/IEC 60601, ISO 26262, UL1998, DO-178B, MIL-STD-882-E, …)
5. legal aspects (insurances, liability, ...)
6. Reputation !

HW-Development Workflow

Simplified process of HW-development:



- Documentation
- Logik synthesis
- Goods managment

Terms #1

test method = test procedure

EMC = Electromagnetic Compliance
SI = Signal Itegrity

CUT = Chip Under Test
UUT = Unit Under Test
DUT = Device Under Test

PCBA (Printed Circuit Board Assembly) = Board

device = case/housing + PCBA + wiring + controls

system = several devices + interconnections

Terms #2

The absence of a quality feature

or

its deviation from a required value
beyond a range of tolerance

is referred to as

FAULT or DEFECT *.*

[Kärger 85]

Where do faults arise ? #1

1. take over of goods, storage, packaging, provision of goods, transport
2. manufacturing of the bare PCB
3. preparation of parts (storage conditions, temperature, moisture, …)

4. Assembly
   - wrong/missing parts
   - wrong orientation/polarity
   - bent leads or pins
   - reduced solderability of leads, pins, pads, wires
   - ESD (Electrostatic Discharges)

http://www.blunk-electronic.de/pdf/esd.pdf

Where do faults arise ? #2

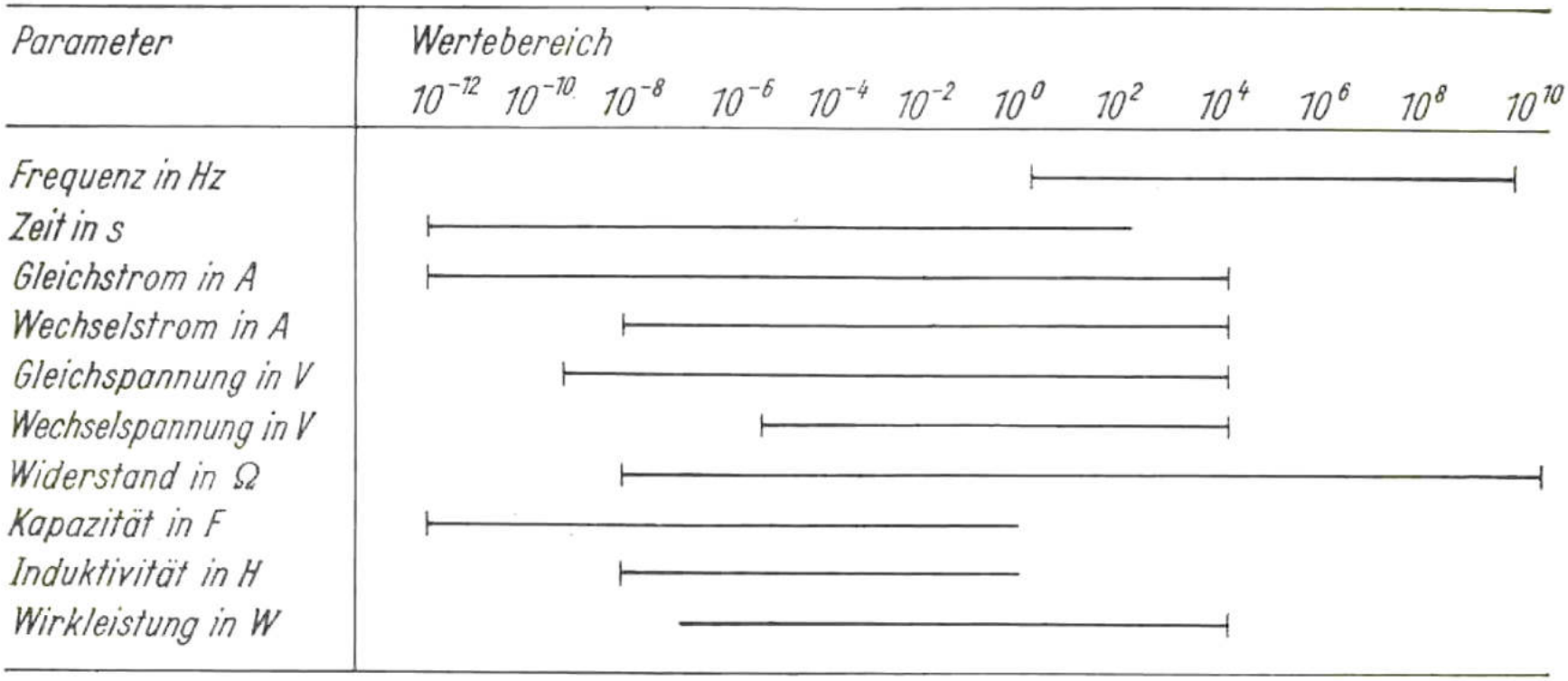
1. Soldering
   - mech. stress of pads and pins due to twisting of the PCB
   - chem. stress due to gasses of soldering flux agents
   - non-optimal soldering process (reflow temperature profile)

2. Wiring / cabeling

3. Test methods and measurement itself
   - inappropriate method
   - tolerance band too narrow
   - misinterpretation of readouts and reports
   - operator errror

What and how accurate do we test ?

1. electrical values [Kärger,85]



2. mechanical values (length, angle, acceleration, velocity, pressure, ...)
3. optical values (brightness, wavelength, dispersion, exit angle, ...)

Classification of Faults

Fehler								
Klassifikationsmerkmal								
Phase des Produktions-prozesses	Charakter des Auftretens	Kausale Verknüpfung	Fehler-wirkung	Fehlerart	Fehlerzahl	Zeitliche Dauer der Fehlerwirkung	Betriebsart des Erzeugnisses	Fehler-gewicht
Entwicklungs-; Konstruk-tions-fehler	grobe	Primär-fehler	Funktions-fehler	Bauelemente-fehler	Einzel-fehler	ständige Fehler	statische Fehler	über-kritische Fehler
Fertigungs-fehler	systema-tische	Folge-fehler	Parameter-fehler	Kontakt-fehler	Mehrfach-fehler	inter-mittierende Fehler	dynamische Fehler	kritische Fehler
Betriebs-fehler	zufällige	Final-fehler		Verbin-dungs-fehler				Neben-fehler
				Bestük-kungs-fehler				unwesent-liche Fehler

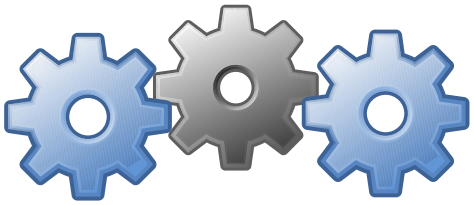
[Kärger,85]

Disturbances in Manufacturing

Unzulänglichkeiten der Erzeugnisentwicklung und Fertigungsvorbereitung	Unzulänglichkeiten der technologischen Verfahren	Unzulänglichkeiten der technologischen Ausrüstung	Mängel der Ausgangsprodukte	Subjektive Mängel der Arbeitskraft	Umwelteinflüsse
Grenzbetrieb Überlastung Unterlastung Arbeitspunkt Aussteuerung Stabilitätsreserve Grenzfrequenz Einschwingzeit Übersprechen parasitäre Kapazitäten, Induktivitäten Leckströme Isolation	Rückstände Nebenwirkungen thermische, mechanische, chemische, elektrische Beanspruchung	Positioniergenauigkeit Bearbeitungsgenauigkeit Dosiergenauigkeit Vibration Schwingen Bearbeitungsdauer Einwirkzeit	Überlagerung Korrosion Lötbarkeit Benetzbarkeit Konzentration Dichte Reinheit Deformation Parametertoleranzen	Verstöße Unachtsamkeit Denkfehler Gedächtnisfehler Konzentrationsschwäche Ermüdung Unlust Emotionen Qualifikation Einarbeitung psycho-physiologische Anpassung	Druck Temperatur Staub Feuchte Gase Aerosole Licht Strahlung

[Kärger,85]

Place of Testing



1. after manuf. steps which add new features
2. when the system level increases (PCB → PCBA → device → system)
3. critical parts (dubious source, varying quality, high price)
4. after fault-intensive procedures (heat, vibration, ...)
5. before labor-intensive steps (assembly)
6. before steps which cover faults/shortcomings
7. before steps which do not allow repairment afterward (moulding, casting, coating, filling, ...)
8. ...

[Kärger,85]

Time of Tests

1. jedes Produkt / Stückprüfung → 100%
2. periodisch
3. Stichprobe

Depends on:

- application and safety level of the product (medical, transportation, military, ...).

- Reliability of manufacturing process

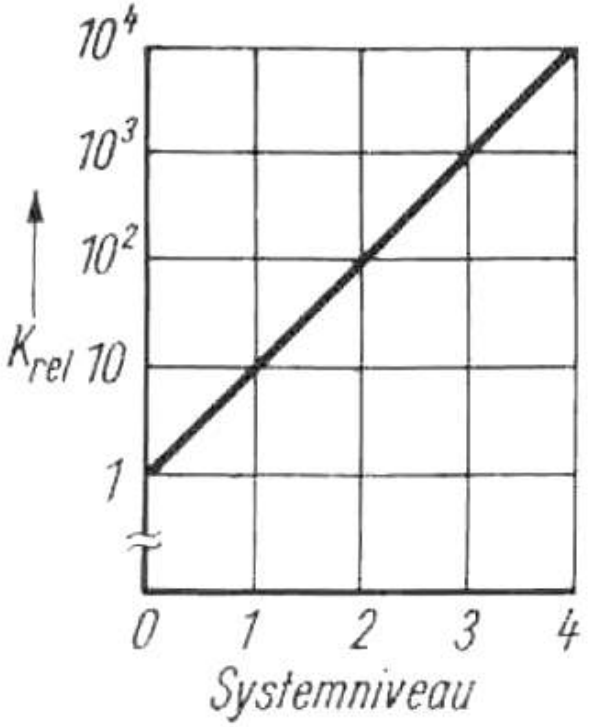
- Sources of parts

Costs for Repair and Rework

Relative costs increase with system level !

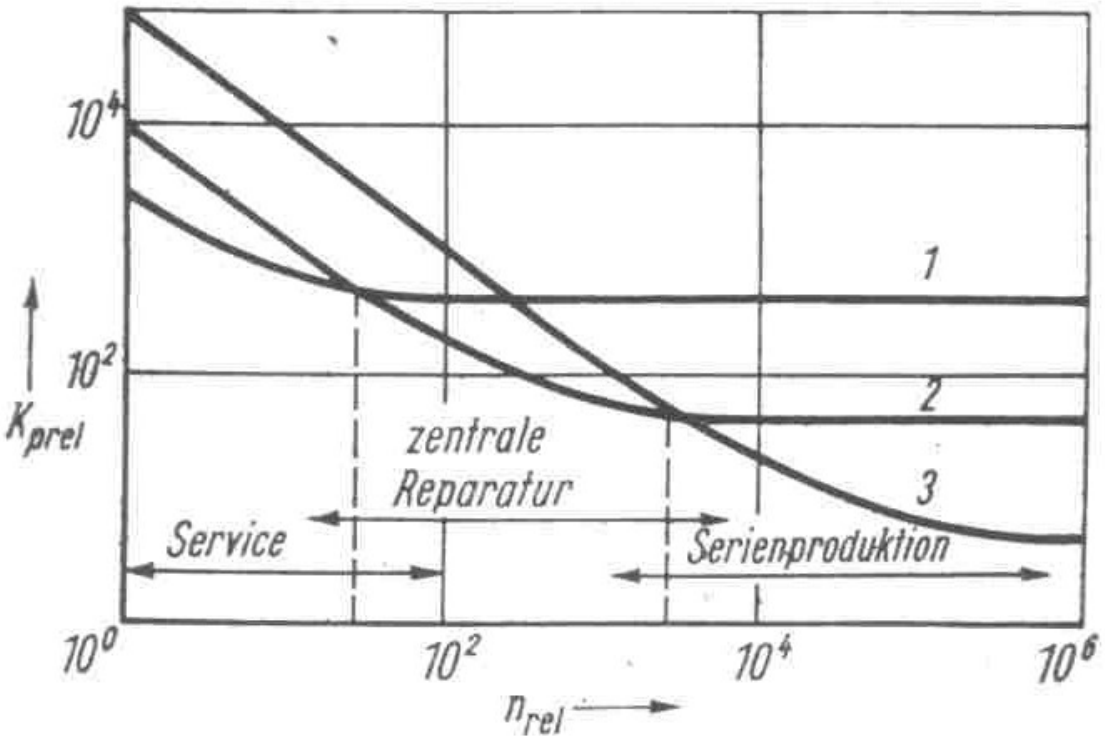
s = 0 single part (R, C, L, T, IC, ...)
s = 1 Submodul
s = 2 Module
s = 3 Device
s = 4 Anlage / System
s = 5 Customer

$$C_{rel} = 10^{s}$$



[Kärger,85]

Costs for Test and Measurement



1 Prüfung mit universellen Prüfmitteln
2 spezielle Prüfplätze
3 Prüfautomaten

[Kärger,85]

Criterions for Test Methods

1. destroying / non-destroying
2. test duration, cycle time
3. accuracy, reliability of the method
4. universality, flexibility (adaption to the UUT)
5. constructive, energetic, economic parameters
6. demand of employees
7. degree of automation (ratio of automated to manual steps)

less automation →
higher qualification of personell →
higher labor costs !

8. reliability testing required (MTBF, MTTF, MTTR) ?

[Kärger,85]

Test Methods Overview #1

- manual visual inspection (MVI)
- automatic optical inspection (AOI)
- automatic X-ray inspection (AXI)
- Solder paste inspection (SPI)
- Infrared termometry (IRT)

- In-Circuit-Test (ICT)
- Flying-Probe-Test (FPT)
- Boundary Scan Test (BST / JTAG / IEEE1149.x)

  (even for system tests !)
- self test (BIST/ BIT)
- function test (FT)

Consider test order and place in manufacting process !

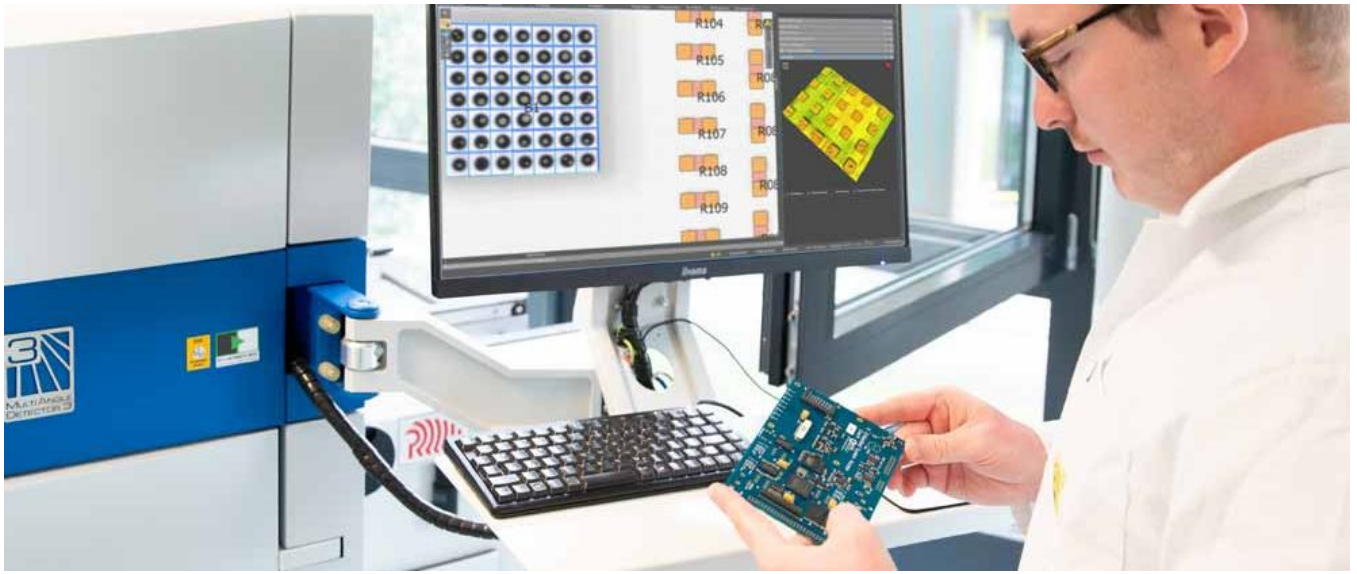
Test Methods Overview #2

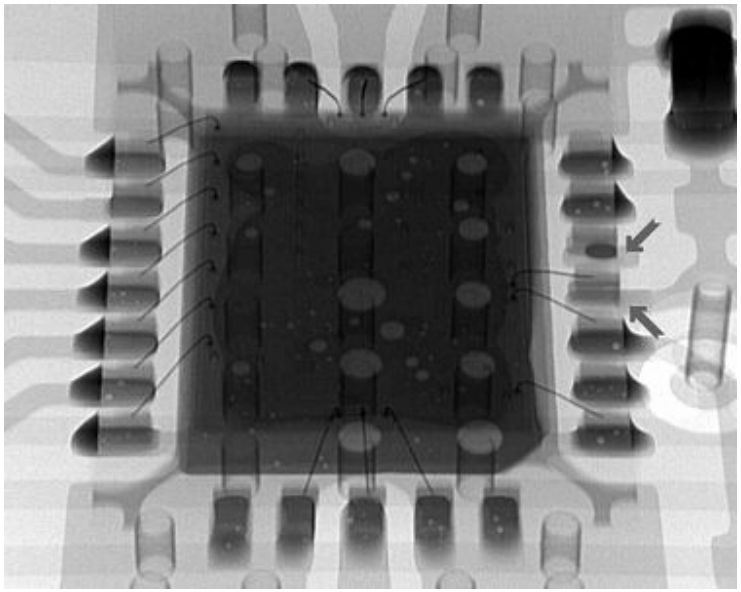
AOI – Automatic Optical Inspection

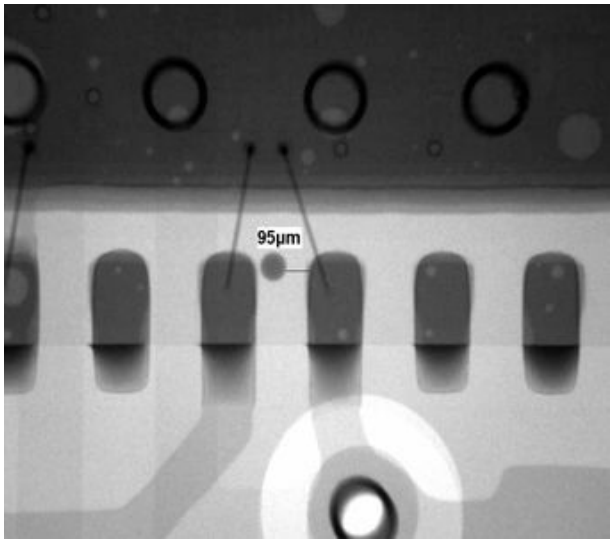
Source: www.goepel.com

Test Methods Overview #3

AXI – Automatic X-Ray Inspection



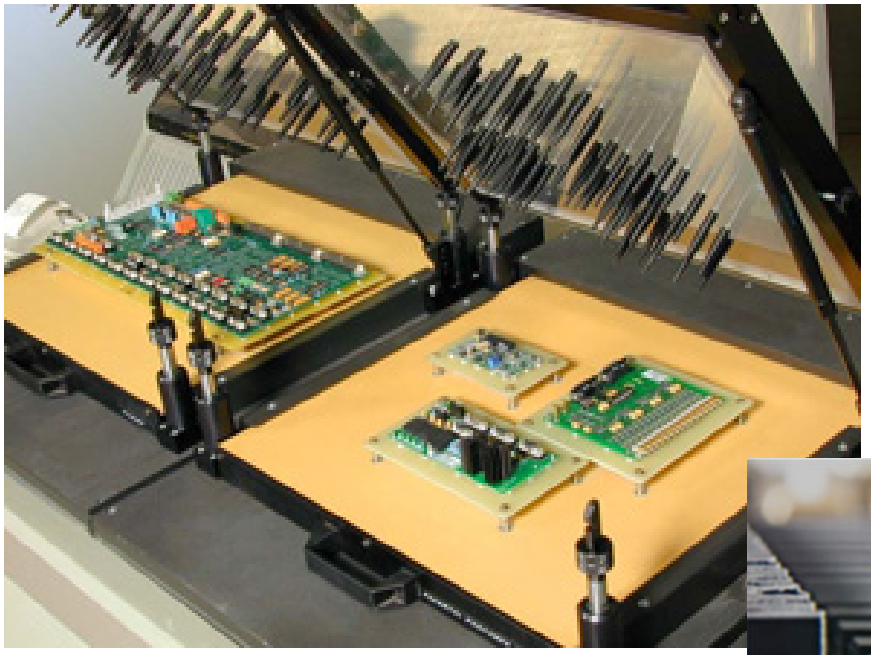




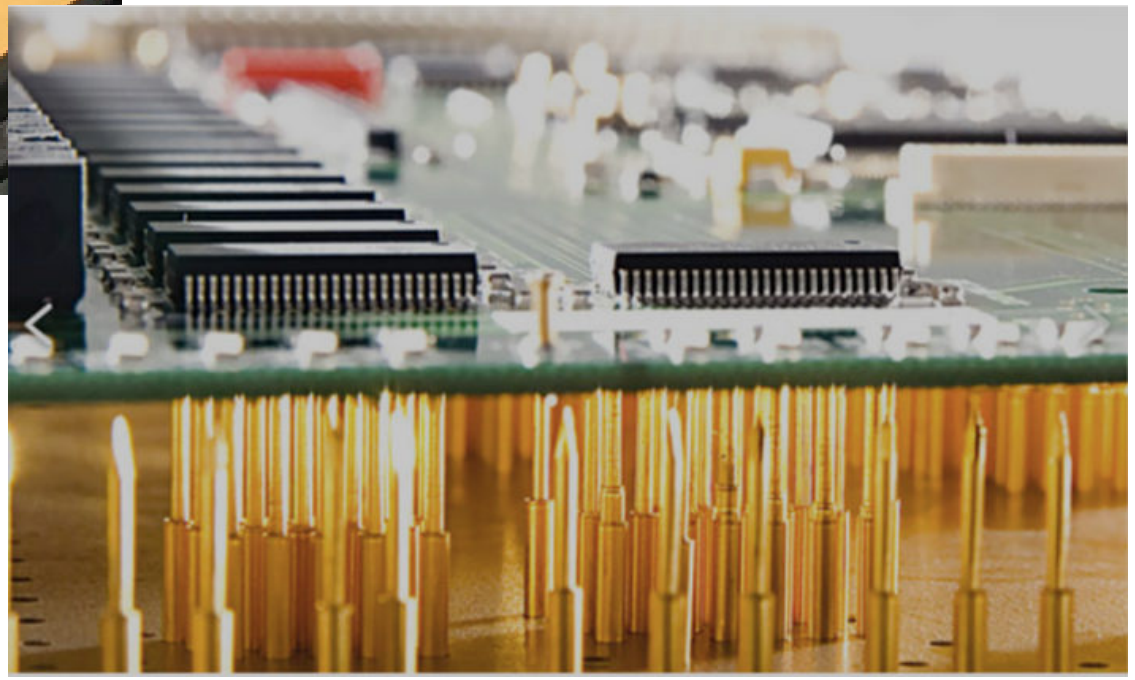
Source: www.goepel.com

Test Methods Overview #4

ICT– In-Circuit-Test



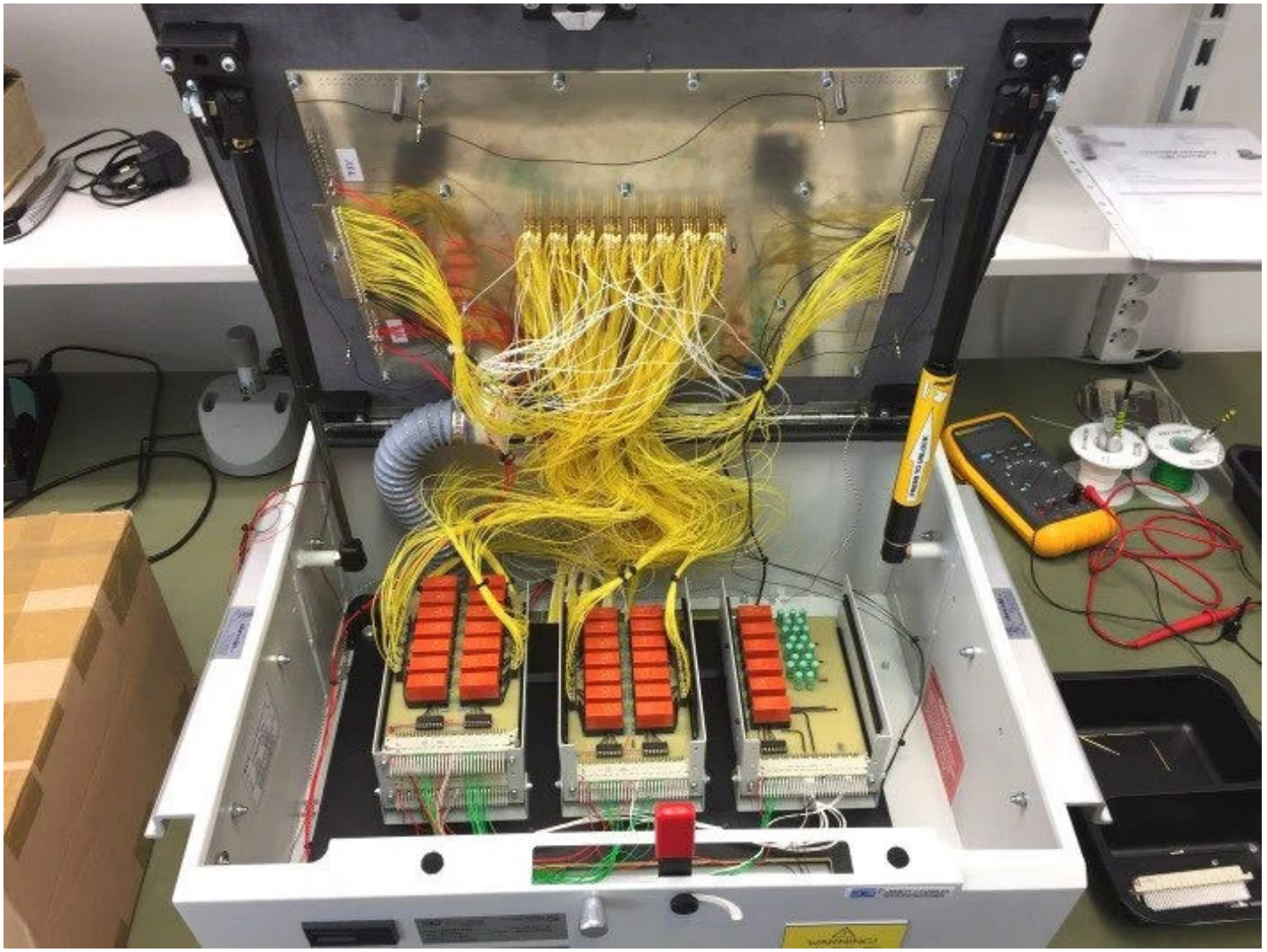
Source: https://www.seica.com



Source: www.altium.com

Test Methods Overview #5

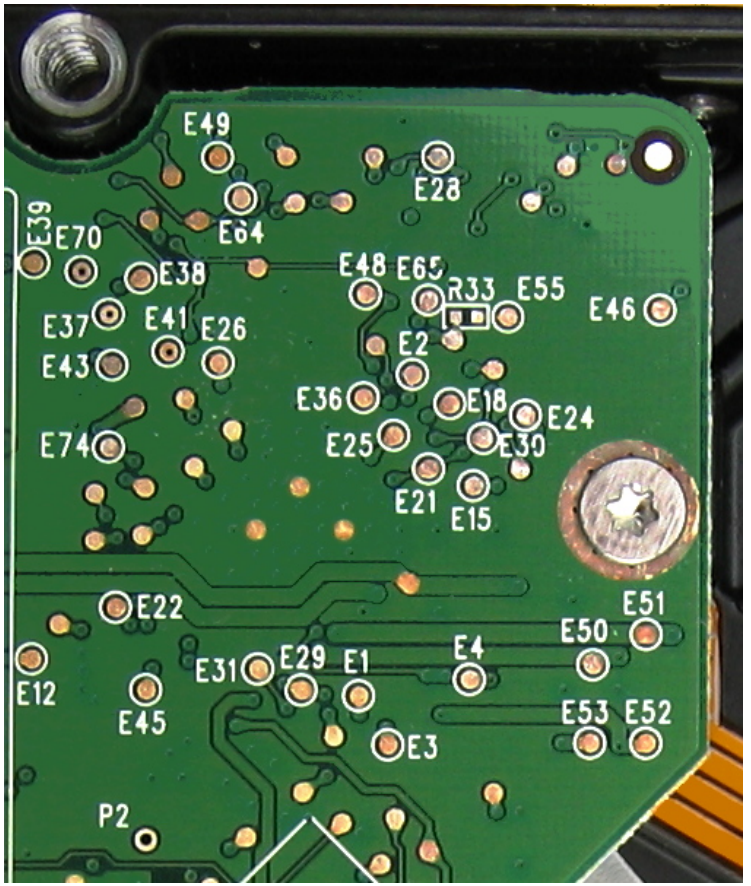
ICT– In-Circuit-Test



Source: https://www.ednasia.com

Test Methods Overview #6

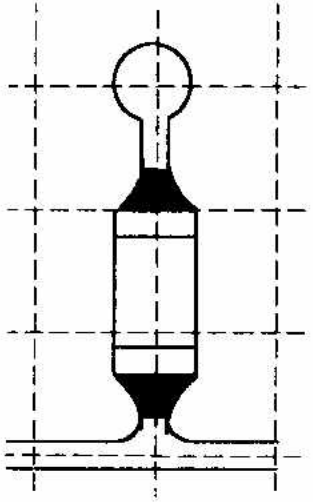
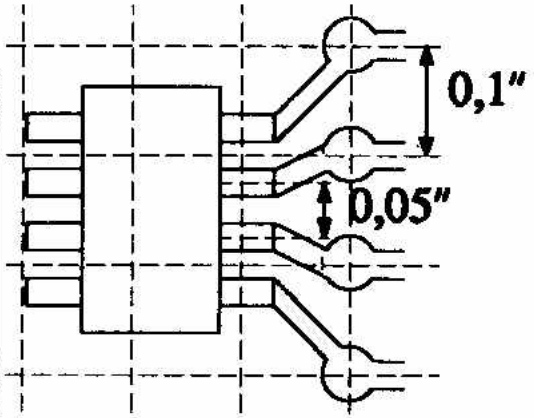
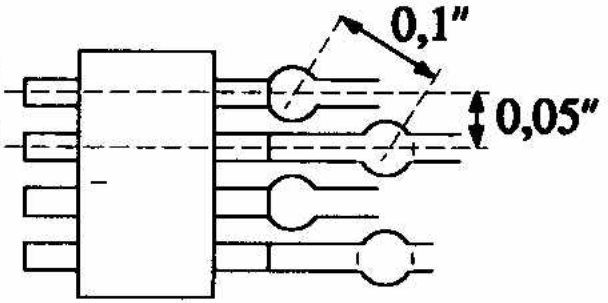
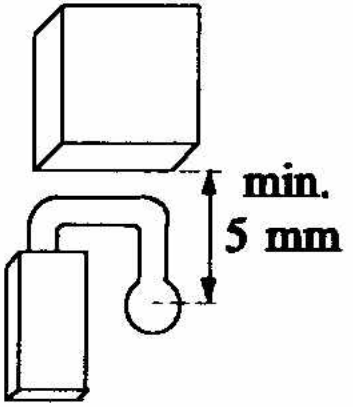
ICT– In-Circuit-Test



Source: https://de.wikipedia.org/wiki/Testpunkt

Test Methods Overview #7

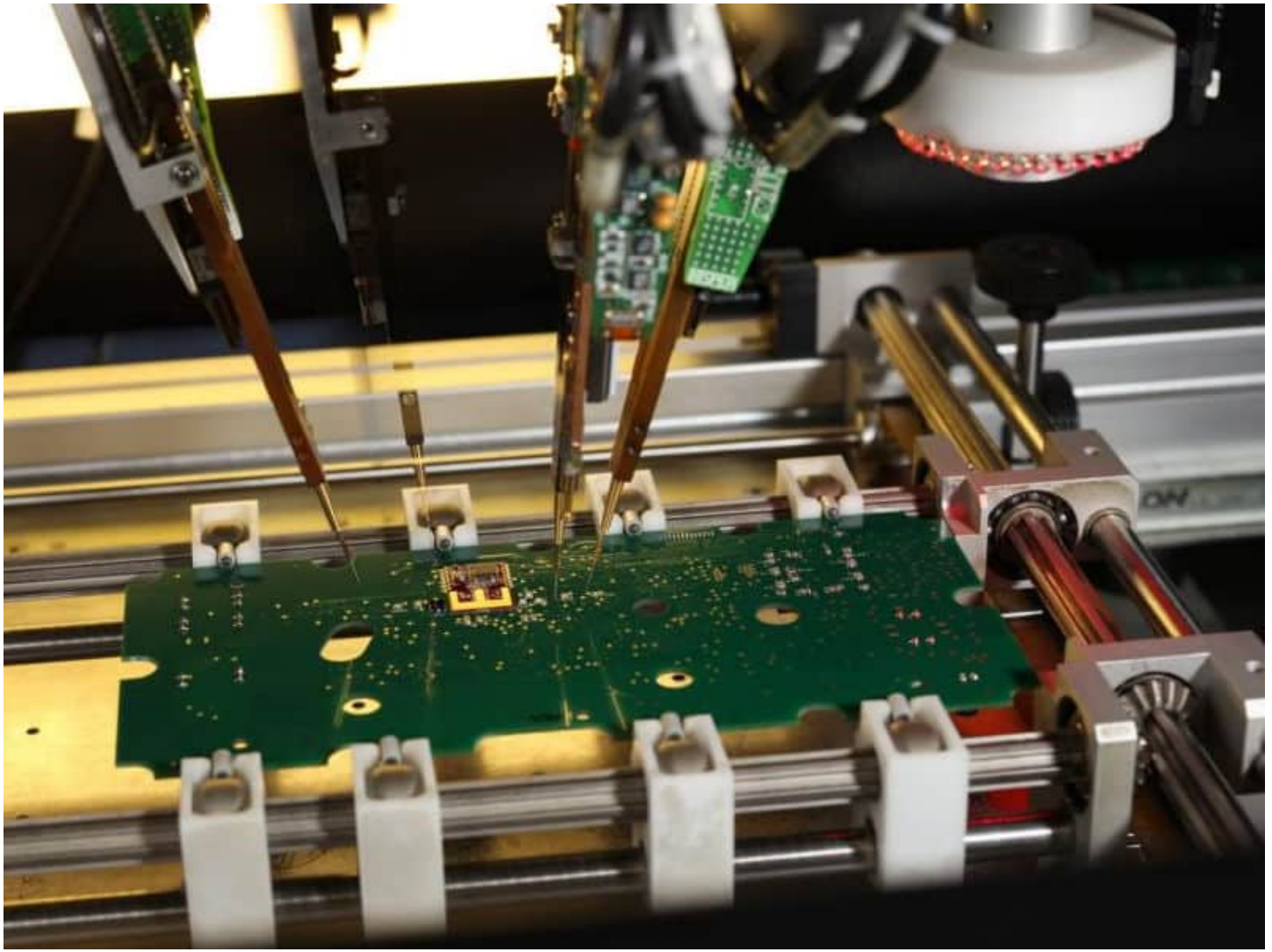
ICT– In-Circuit-Test

Kontaktierungs-fläche	gefächerte Kontaktierungsflächen	versetzte Kontaktierungsflächen	Abstand von hohen Bauteilen
			

[Kärger,96]

Test Methods Overview #8

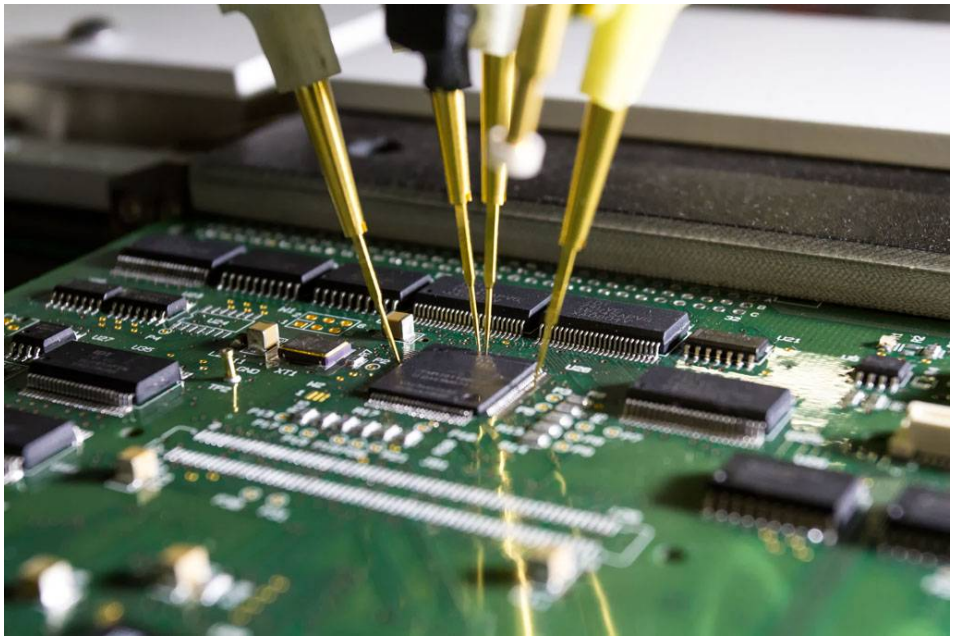
FPT – Fying-Probe-Test



Source: https://hillmancurtis.com

Test Methods Overview #9

FPT – Fying-Probe-Test



Source: https://www.q1testinc.com

Source: www.spea.com

Application of Test Methods #1

Method	Application	Remarks
visual inspection / MVI	- superficial to sophistical **optical** inspection of PCBA, devices and systems - may be economical with low volume production (space, avionics, MIL, medical, transportation, safety critical applications, ...)	- depends on human condition - time requirement very low to very high
AOI	fast, sophistical, automatic **optical** inspection of PCBA	- sophistical, expensive machinery required
AXI	fast, sophistical, automatic **optical** X-ray inspection of PCBA	- sophistical, expensive machinery required
IRT / thermal imaging	detection of thermal stress	- for reliability tests

Application of Test Methods #2

Method	Application	Remarks
ICT	fast, sophisticated **electronical** test of PCBA	extensive mechanical adaption to a UUT
FPT	moderately time requiring **electronical** test of PCBA	flexible mechanical adaption to many UUT
BST	very fast, sophisticated, **electroical** test of PCBA, devices and systems	mainly for digital circuitry of the UUT
BIST / BIT	very fast, sophisticated, **electroical** test of PCBA, devices and systems	- expenses during development - minimal functionality of the UUT mandatory
function test / FT	- superficial **electrical** test of PCBA, devices and systems - test of peripherals	low inspection depth, less detailed fault diagnosis

Fault Detection / Test Coverage #1

Fehlerarten	Sichtkontrolle	AOI (2D)	AOI (3D)	AXI	Boundary Scan	MDA (analoger ICT)	In-Circuit-Test (ICT)	Funktionstest
Bestückung analog:								
Bauelement fehlt	++	++	++	++	-	++	++	+
Stützkondensator/Hf-Bauelement fehlt	++	++	++	++	-	-	-	-
Bauelement falsch	+	+	+	-	-	++	++	+
Bauelement verpolt	++	++	++	-	-	++	++	+
Elko verpolt	++	++	++	+	-	+	+	-
Tantalkondensator verpolt	++	++	++	-	-	-	-	-
Bestückung digital:								
IC fehlt	++	++	++	++	+	++	++	++
IC falsch	++	+	+	-	+	-	++	++
IC verpolt	++	++	++	-	+	-	++	++

Legende: ++ sehr gut testbar, + nur teilweise testbar, - nicht testbar

https://www.elektronikpraxis.vogel.de/die-wichtigsten-design-for-test-regeln-fuer-elektronische-baugruppen-a-95416/

Fault Detection / Test Coverage #2

Fehlerarten	Sichtkontrolle	AOI (2D)	AOI (3D)	AXI	Boundary Scan	MDA (analoger ICT)	In-Circuit-Test (ICT)	Funktionstest
Lötfehler:								
Open analog	++	++	++	++	-	++	++	+
Open digital	++	+	++	++	+	++	++	+
Open BGA	-	-	-	++	++	++	++	+
Short analog	++	+	+	+	-	++	++	+
Short digital	++	+	+	+	+	++	++	+
Short BGA	-	-	-	++	++	++	++	+
unvollständig (Meniskus)	++	+	++	++	-	-	-	-
Solder Balls	+	-	-	-	-	-	-	-
Bauelemente-Fehler:								
analoge Bauelement defekt	-	-	-	-	-	++	++	+
IC defekt	-	-	-	-	+	-	++	++
Bauelement mechanisch defekt	++	-	-	-	-	-	-	-
Funktionsfehler	-	-	-	-	+	-	-	++
Bauelemente versetzt	+	++	++	+	-	-	-	-

Legende: ++ sehr gut testbar, + nur teilweise testbar, - nicht testbar

https://www.elektronikpraxis.vogel.de/die-wichtigsten-design-for-test-regeln-fuer-elektronische-baugruppen-a-95416/

Optical / Visual Tests

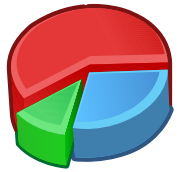
Place in the manufacturing process: previous to electrical tests

Device and system tests

detectable faults:

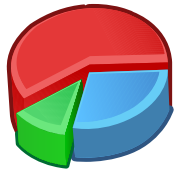
- missing connection (wire, solder, screw, …)
- short-circuit (wires, solder, …)
- shortcomings of the connection (solder, wire wrap, …)

Visual Inspection / MVI #1



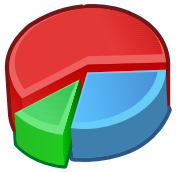
Pros	Cons
minimal equipment: loupe, light, fixture, ...	Quality depends on the condition of the human being.
fast „adaption“ to the UUT (checklist)	
no electrical or thermal stress for the UUT	UUT must be handled, touched, transported, moved (danger of dropping, ESD, ...)
wrong position, orientation, polarity of parts can be detected	no clear assertion with regard to the functionality of the UUT
integration with Boundary-Scan (BST possible	writing and archiving test reports cumbersome and slow (checklist)

Visual Inspection / MVI #2



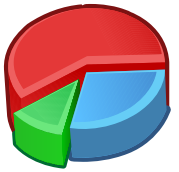
Notes

AOI #1



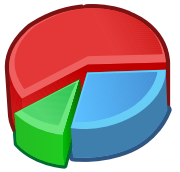
Pros	Cons
test quality constant (machinery does not get tired)	expensive machinery (70-100T EUR)
no electrical, thermal or mechanical stress to the UUT	moderate time required for settiung up the test program (appr. 24h)
low test duration (seconds to minutes)	visible light → obscured solder joints and parts can **not** be inspected (RF-shielding)
wrong position, orientation, polarity of parts can be detected	no clear assertion with regard to the functionality of the UUT
integration with Boundary-Scan (BST) possible	
automated creation and archiving of test reports	during development placing of parts must be considered (dead angle, …) → DFT

AOI #2



Notes

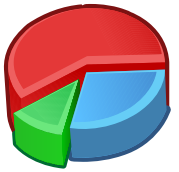
AXI #1



Pros	Cons
test quality constant (machinery does not get tired)	expensive machinery (>100T EUR)
no electrical, thermal or mechanical stress to the UUT	moderate time required for settiung up the test program
low test duration (seconds to minutes)	inspection of lead-free solder more difficult than leaded solder (density 20% lower)
wrong position, orientation, polarity of parts can be detected	no clear assertion with regard to the functionality of the UUT
integration with Boundary-Scan (BST) possible	
automated creation and archiving of test reports	overlapping objects difficult to distinguish
inspection of obscured objects (BGA pads, casting, inner signal layers, ...)	

https://pdfs.semanticscholar.org/ba9a/aeda85a6b3a1ac966b950b36c7078c54f645.pdf

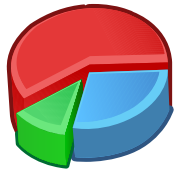
AXI #2



Notes

https://www.youtube.com/watch?v=GhL-ULXowG8

Infrared Thermal Imaging IRT #1

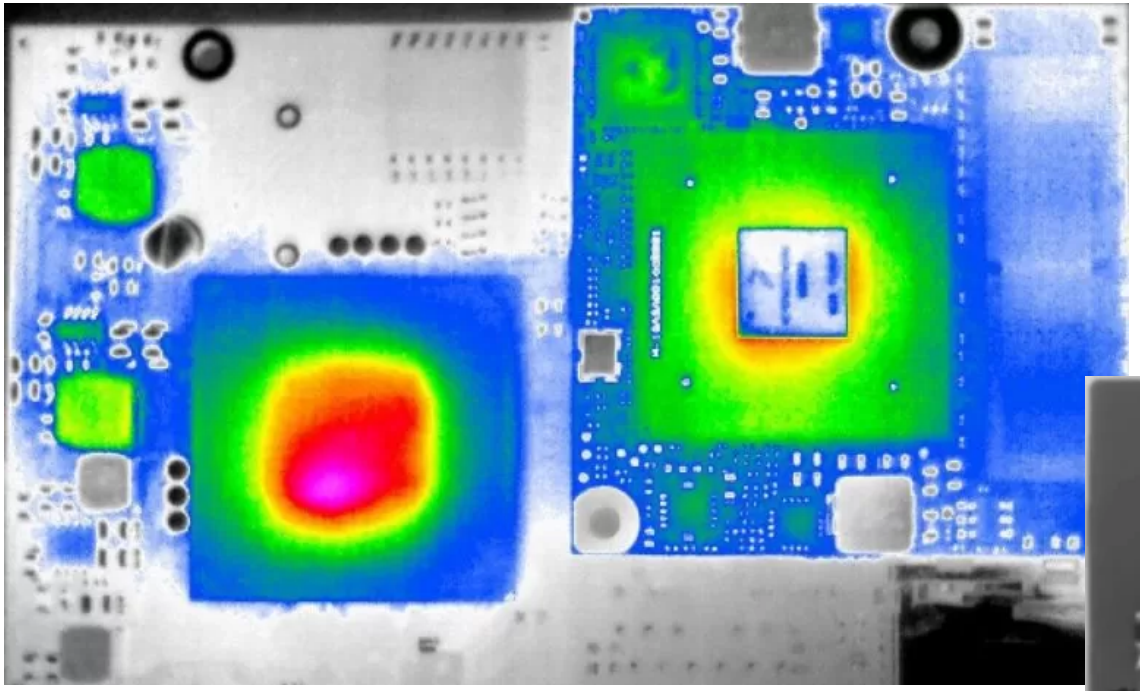


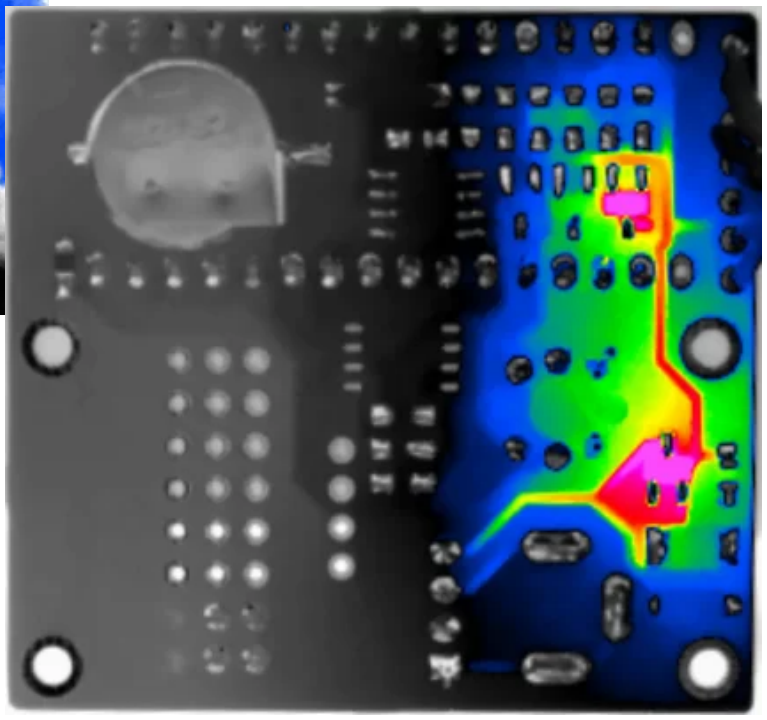
Pros	Cons
detection of thermal stress (single parts, PCB, ...)	UUT is electrically and thermally stressed
assertion to heat distribution, temperature profile	sophisticated infra-red-camera required
for reliabilty analysis interesting (failure rate increases with temperature)	color and material of the objects have influence on the temperature measurement. (emissivity)
	time consuming

Notes

[Kärger, 85]

Infrared Thermal Imaging IRT #2





Quelle: https://workswell-thermal-camera.com/pcb-inspection-by-thermal-imaging/

Electric/Electronic Tests

place in the manufacturing process:	after optical tests/inspections
level:	PCBA, device, system
structural test:	interconnections, parts, pads/pins, values of parts (resistance, capacitance, tolerances, ...)
system tests:	PCBA, device, system
static faults:	current consumption too low/high stuck-at, open, short
dynamic faults:	delays, rise-time, fall-time, response to load surges/dumps, regulation time, ...

Characteristics To Be Tested #1

	gain	characteristic curve	bandwidth, cut-off frequency	harmonic distorsion	noise	phase distorsion	zero point	offset voltage	input current	intput impedance	output impedance	supply voltage	current consuption	output power	settle time	stability, drift	degree of modulaton	sensitvity	output voltage	output current	ripple voltage	conversion time	monotony / linearity	hysteresis	threshold voltage	delay
amplifier	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x										
generator				x	x	x					x	x	x	x	x	x										
modulator		x		x	x							x	x				x									
receiver	x	x	x	x	x							x	x			x		x								
demodulator		x		x	x							x	x						x							
power supply											x	x	x	x	x	x			x	x	x					
transverter													x	x		x			x	x	x					
DA/AD converter		x			x		x	x		x	x	x	x			x		x	x			x	x			
multiplier		x		x	x											x			x							
comparator	x		x					x	x				x						x					x	x	x

[Kärger, 85]

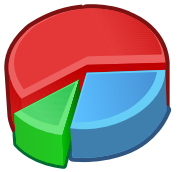
Further Characteristics #2

- protection against touching of normally live parts
- insulation fault current
- protection against arising of shorts and against damages resulting thereof
- overvoltage/overcurrent protection
- heat/fire protection
- isolation resistance
- moisture
- clearance, creepage
- mechanical shock, vibration, acceleration
- temperatur (static, dynamic, cycling)
- ionizing radiation (EM, neutrons, beta, gamma, ions, ...)
- aerosols, salt, gasses, …
- biological influence (mold, insects, dust, ..)

- ESD
- failure rates (MIL-HDBK-217, ANSI VITA 51.x, AEC-Q ?, ...)

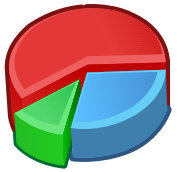
https://electrical-engineering-portal.com/electric-shock-protection-earthing-systems-rcds

ICT #1



Pros	Cons
test quality constant (machinery does not get tired)	expensive machinery
UUT is stressed electrically and mechanically.	moderate time required for setting up the test program (24h)
low test duration (seconds to minutes)	no clear assertion with regard to the quality of solder joints
covers digital & analog circuitry (mixed signal)	no clear assertion with regard to positioning, orientation, polarity of some components (capacitors)
In-System Programming (ISP) possible (increases test duration)	Testpads must be provided on the PCB during development. Parasitic capacitance. Extra space required. → DFT
very detailled diagnosis down to part and net level → minimal costs for repair	expensive mechanical and electrical adaption for just one kind of UUT ! Custom “bed-of-nails” fixture.

ICT #2



Pros	Cons
integration of Boundary-Scan Test (BST) possible	almost no way to update/modify adaption (wiring, test nails, ...)
low risk of operator errors during test mode (assembly line)	inductive and capacitive load of the signals of the UUT
labor costs moderate for test-mode (assembly line)	Back-driving may cause stress to components (wear-out ?)
automated creation and archiving of test reports	no device and system test possible
	obscured solder joints and nets can **not** be tested (BGA, inner signal layers, ...)
	high costs for test program development

ICT #3

Limitations of ICT:

- very low capacities, inductivities, resistances → MVI / AXI / AOI
- RF, Signal Integrity (SI), reflections
- „high voltage / high current“ (relative)
- very low voltages, low currents (µV, nA)
- „Feedback“ LEDs, displays, swiches, push-buttons, ...

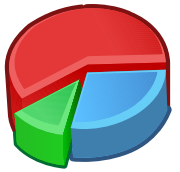
Other kinds of ICT:

- Manufacturing Defect Analyzer (MDA) – a reduced ICT with limited component diagnostic capability. See https://www.optimatech.net/knowledge-center/manufacturing-defect-analyzer-testing.aspx

- Cableform Tester
  See https://www.insys-test.de/kategorie/kabelbaumtester/

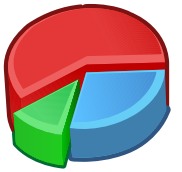
  https://www.youtube.com/watch?v=ixUJRRBt4YQ

FPT #1



Pros	Cons
test quality constant (machinery does not get tired)	very expensive machinery (200-500T EUR)
UUT is stressed electrically and mechanically.	moderate time required for setting up the test program
moderate test duration (minutes)	
covers digital & analog circuitry (mixed signal)	no clear assertion with regard to the quality of solder joints
integration of Boundary-Scan Test (BST) possible	no clear assertion with regard to positioning, orientation, polarity of some components (capacitors)
very detailled diagnosis down to part and net level → minimal costs for repair	Testpads must be provided on the PCB during development. Extra space required. → DFT

FPT #2



Pros	Cons
fast „adaption“ to UUT	obscured solder joints and nets can **not** be tested (BGA, inner signal layers, ...)
low risk of operator errors during test mode (assembly line)	inductive and capacitive load of the signals of the UUT
labor costs moderate for test-mode (assembly line)	high costs for test program development
automated creation and archiving of test reports	no device and system test possible
	- noise emission - operator exposured to noise

FPT #3

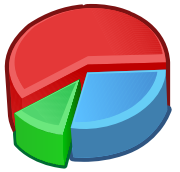
Limitations of FPT:

- very low capacities, inductivities, resistances → MVI / AXI / AOI
- RF, signal integrity (SI), reflections
- „high voltage / high current“ (relative)
- very low voltages, low currents (µV, nA)
- „Feedback“ LEDs, displays, swiches, push-buttons, ...

https://www.youtube.com/watch?v=sj5yDyWw67w

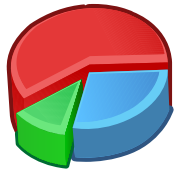
https://www.youtube.com/watch?v=retGdoV-IlQ

BST #1



Pros	Cons
test quality constant (machinery does not get tired)	moderate costs for equipment (5-50T EUR)
UUT may get stressed electrically on fault (Be cautions with the debugger !).	moderate time required for setting up the test program (1 to 5 days)
very low test duration (seconds)	Support-intensive. High cost for test program development.
In-System Programming possible (increases test duration)	no clear assertion with regard to the quality of solder joints
covers mainly **only digital** circuitry (IEEE 1149.1 / 6 / 7).	**analog** circuitry can **not** be tested (limited access to ADC, DAC), IEEE 1149.4 ?
very fews test pads or extra connectors required	Power supply must be provided and monitored (current consumption).
very detailled diagnosis down to part and net level → **moderate** costs for repair (skills on schematic design required)	

BST #2



Pros	Cons
reuse of equipment for „adaption“ and wiring	Circuitry required for test must be implemented during design. → DFT
rapid modification of test program (minutes).	no clear assertion with regard to positioning, orientation, polarity of some components (capacitors). Risk of immediate damage on power-up. → optical inspection
low labor costs in test-mode (assembly line)	interaction with operator required when switches, LEDs, displays, … are to be tested
start-up of prototypes	missing solder joints for **power supply** of ICs (BGA) are not detected → faults in FT
device and system test possible (even in the field !)	**NO clear assertion with regard to quality of solder joints, wiring, ...**
design errors can be detected → DFT	
automated creation and archiving of test reports	

BST #3

Boundary Scan (probing at the boundary) is an adaptorless structural test method that:

1. detects manfuacturing faults down to pin/pad and net level.
2. allows testing of IC, assembled PCBs and systems.
3. enables electrical access to nets and pads which are physically not accessible.
4. reduces the electrical access to the UUT to just 5 signals.
5. test the UUT under full operating voltage.
6. allows in-system-programming (ISP).
7. bases on electronical testpoints embedded in the ICs.
8. is standardized according to IEEE 1149.x (since 1990es).

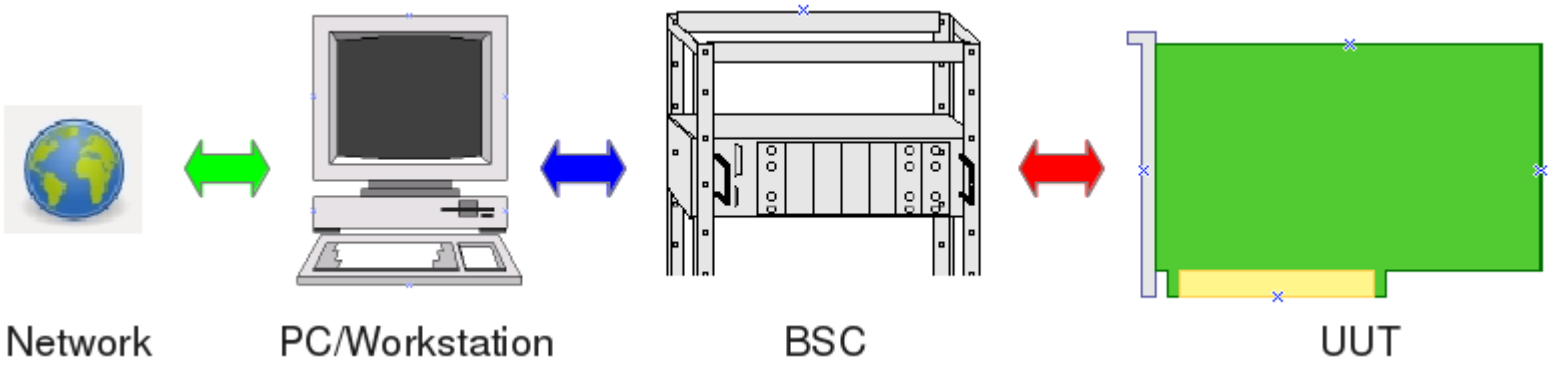
BST #4

Why Boundary Scan ?

1. During development, design errors can be detected (DFT).
2. Manufactuing faults are detected at structural level (shorts, opens, missing or wrong parts).
3. Simplified test of prototypes.
4. Systemtest at structural level (racks, backplanes, units, cables, wiring, …)
5. Simplified and fast repair (debugging).
6. Less mechanical equipment required (no nail-adapter, less functional testing)
7. Fast and automated test program setup (build-processes, scripting, …)
8. Combination with clima test, mechanical stressing, ...

BST #5

System Overview:

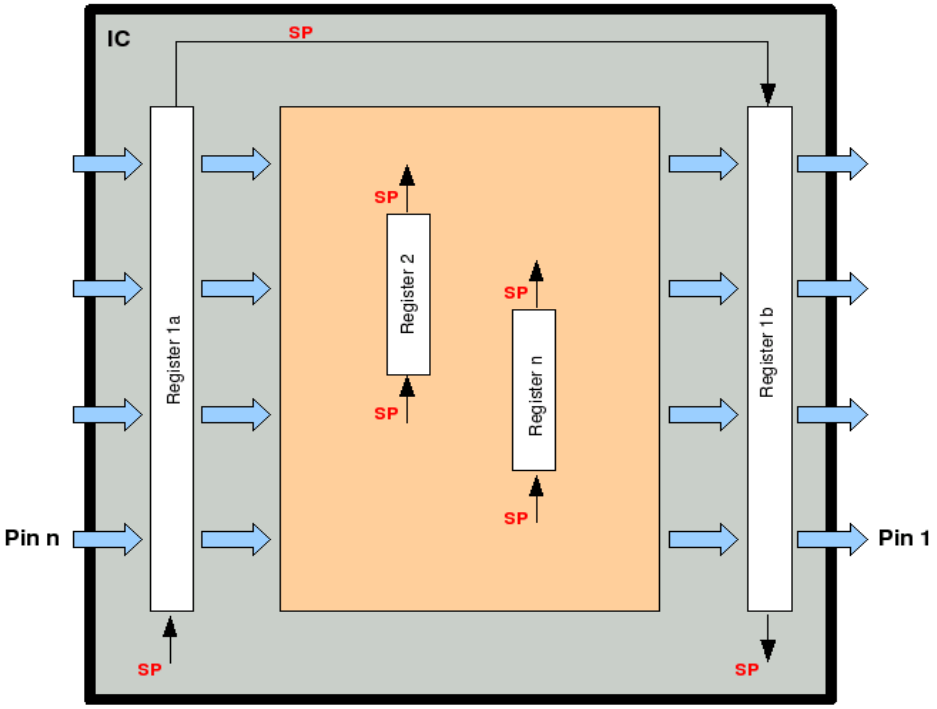


How does it work ?

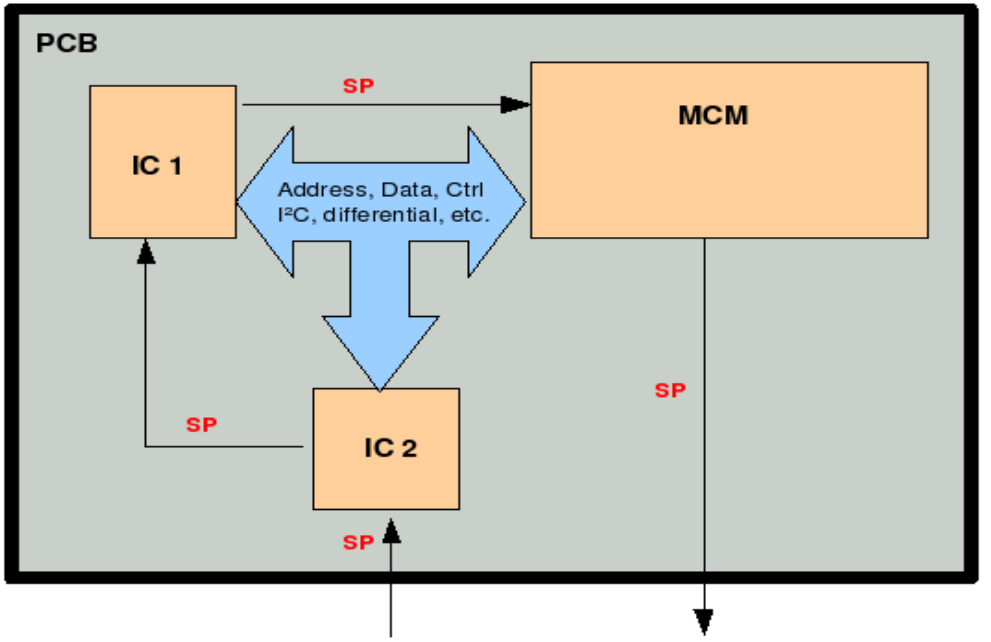
1. Around the actual core logic of an IC (at its boundary) a long digital shift register is wrapped. This register allows read and write access to a pin/pad of the IC.
2. Between ICs, SoC-modules and boards test data flows to and fro.

BST #6

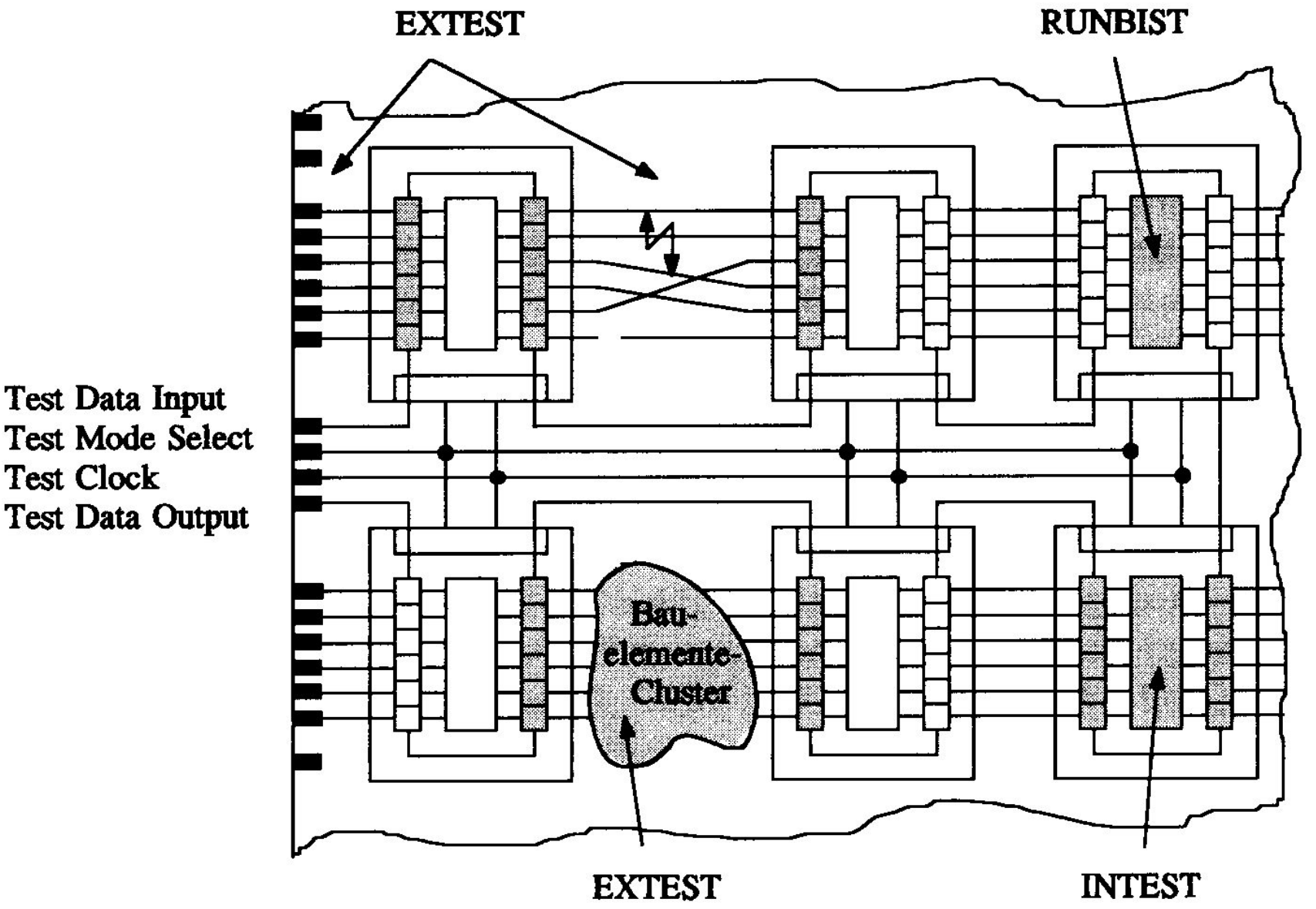
shift register inside the IC
around its core:



interconnections between ICs:



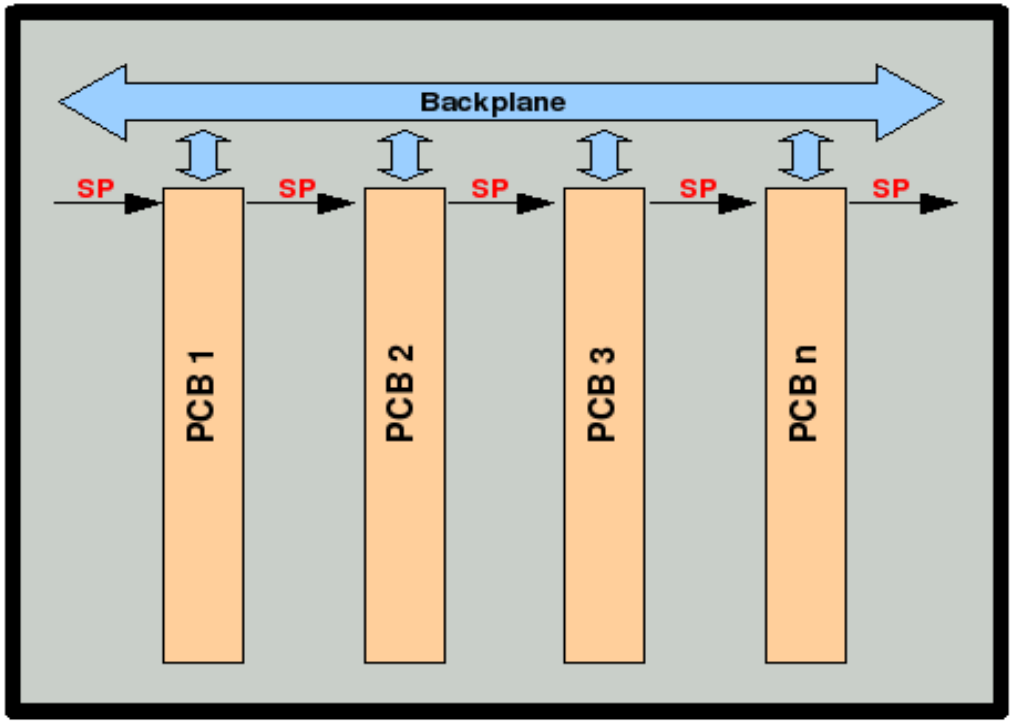
BST #7



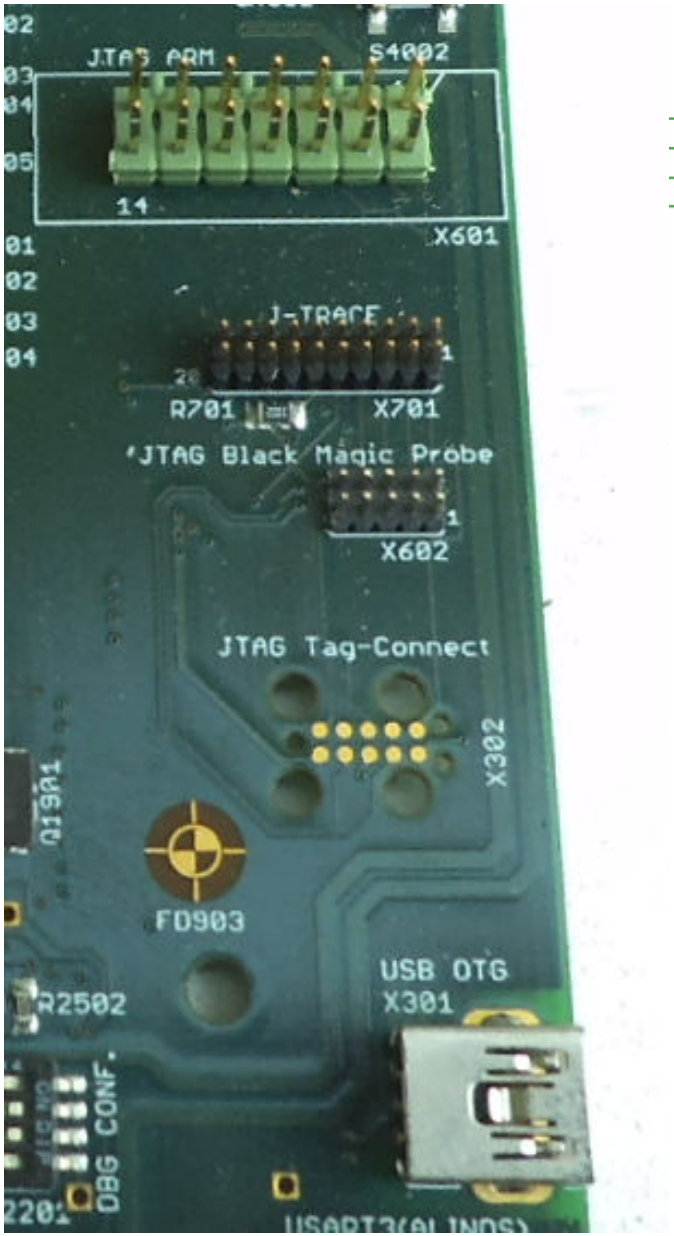
[Kärger,96]

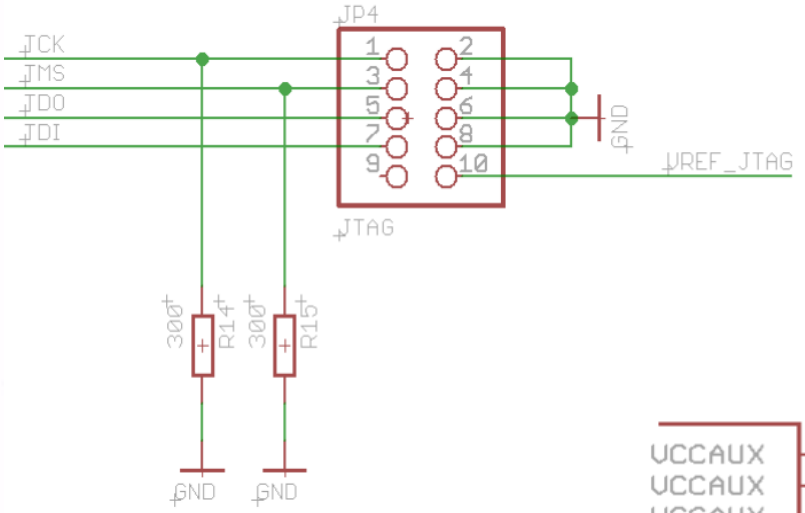
BST #8

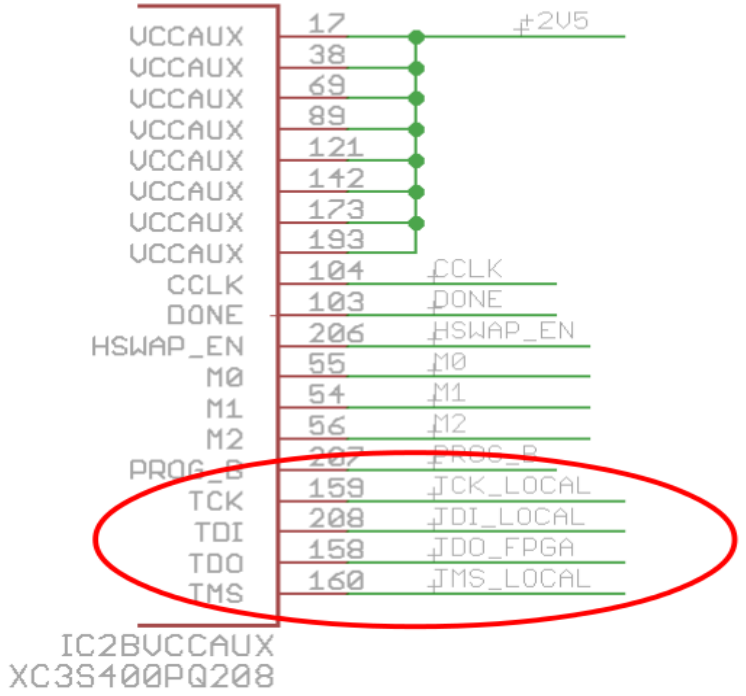
Device and systemtest via
backplane or cableform:



BST #9


JTAG ARM
S4002
14
X601
J-TRACE
R701
X701
*JTAG Black Magic Probe
X602
JTAG Tag-Connect
X302
FD903
USB OTG
X301
R2502
DBG CONF.


JP4
JTAG
TCK
TMS
TDO
TDI
GND
VREF_JTAG
300
R14
R15
GND


VCCAUX
CCLK
DONE
HSWAP_EN
M0
M1
M2
PROG_B
TCK
TDI
TDO
TMS
17
38
69
89
121
142
173
193
104
103
206
55
54
56
159
208
158
160
+2V5
CCLK
DONE
HSWAP_EN
M0
M1
M2
TCK_LOCAL
TDI_LOCAL
TDO_FPGA
TMS_LOCAL
IC2BVCCAUX
XC3S400PQ208

BST #10

Synonoyms:	JTAG / IEEE1149
Place in the manufacturing chain:	- after optical tests/inspections - device and systemtest
Integration in:	MVI, AOI, AXI, ICT, FPT, FT

Limitations (IEEE1149.1/6/7):

- dynamical characteristics (delays, frequency, duty cycle, edges, ..)
- analog circuitry (operational amplifiers, comparators, filters, …)

Specialties:	IEEE 1149.4 (mixed Signal Test)

BST #11

Sub-categories:

1. Infrastructure-test / scanpath-test / scanchain-test
2. Interconnect-test (various algorithms)
3. logic cluster test
4. Memory-connect-test
5. Memory-test (time extensive)
6. Memory-Content-Verification (ROM / FLASH)
7. In-System-Programming (FLASH, SVF, STAPL, IEEE1532, I^2C, SPI, …)
8. Periphery test (LEDs, displays, push buttons, relais, motors, ...)
9. analog cluster (ADC, DAC, ...)

10. Wriring test
11. Module-test
12. System-test

BST #12

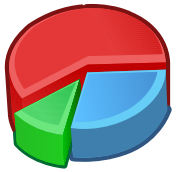
References / Further reading:

1. The Institute of Electrical and Electronics Engineers, Inc. , 3 Park Avenue, New York, NY 100165997, USA; IEEE Std 1149.12001
   "IEEE Standard Test Access Port and Boundary Scan Architecture"
2. Parker, 2015, The Boundary-Scan Handbook

3. http://www.blunk-electronic.de/bsm/Boundary_Scan_Basics.pdf
4. http://www.blunk-electronic.de/bsm/how_to_test.pdf
5. http://www.blunk-electronic.de/bsm/System_M-1_Manual_en.pdf

https://www.youtube.com/watch?v=Y_dfg8h_yEY

Self Test / BIST #1



Pros	Cons
constant test quality	system test → fault diagnosis at high level. Detection of missing parts, faulty solder joints **limited.**
can be run in the whole lifetime of the UUT (not just in the factory)	requires a minimum of functionality of the UUT
time required for the test is minimal → low labor costs	
Expenses for coding the test program in product development phase.	**NO clear assertion with regard to quality of solder joints, wiring, ...**
Few equipment required (power supply, loop-back cables, ...)	wrong positioning, orientation, polarity of some parts can **not** be detected (capacitors). Risk of immediate damages on power-up.
Combination with environmental tests possible	Power supply required. Should be monitored !

Self Test / BIST #2

Operation principle:	- bases on function which have been implemented by design → DFT - triggered and evaluated by external control signals
Level:	IC, PCBA, device, system
Place in the manufacturing chain:	after FPT, ICT, BST, In-System-Programming

Self Test / BIST #3

Sub-Categories:

1. Programmable built-in self-test (pBIST)
2. Memory built-in self-test (mBIST) - e.g. with the Marinescu algorithm[1]
3. Logic built-in self-test
4. Analog and mixed-signal built-in self-test (AMBIST)
5. Continuous built-in self-test (CBIST, C-BIT)
6. Event-driven built-in self-test, such as the BIST done to an aircraft's systems after the aircraft lands.
7. Periodic built-in self-test (C-BIT/P-BIT)
8. Interrupt-driven built-in self-test (IBIST) or user/operator-initiated built-in self-test (I-BIT, or O-BIT)
9. Power-up built-in self-test (PupBIST, P-BIT)
10. Automatic built-in self-test (ABIST)

See: https://en.wikipedia.org/wiki/Built-in_self-test

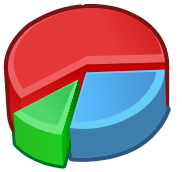
Self Test / BIST #4

Further reading:

1. http://www.eng.auburn.edu/~agrawvd/E6970/LECTURES/chap15.pdf
2. https://en.wikipedia.org/wiki/Built-in_self-test
3. http://www.dtic.mil/dtic/tr/fulltext/u2/a069384.pdf
4. http://www.dtic.mil/dtic/tr/fulltext/u2/a101130.pdf
5. https://pdfs.semanticscholar.org/2d5c/0091610299d10e37426b0a8ae7872e68ee31.pdf

[See Kärger,96]

Function Test / FT



Type	Properties
A	- regulare periphery/accessories incl. power supply connected **- without** external, special test equipment
B	- **monitored power supply** connected - periphery/accessories are simulated **by external** test equipment (ATE)

A UUT is regared as testable, if

- it can be set to a known and stable initial state.

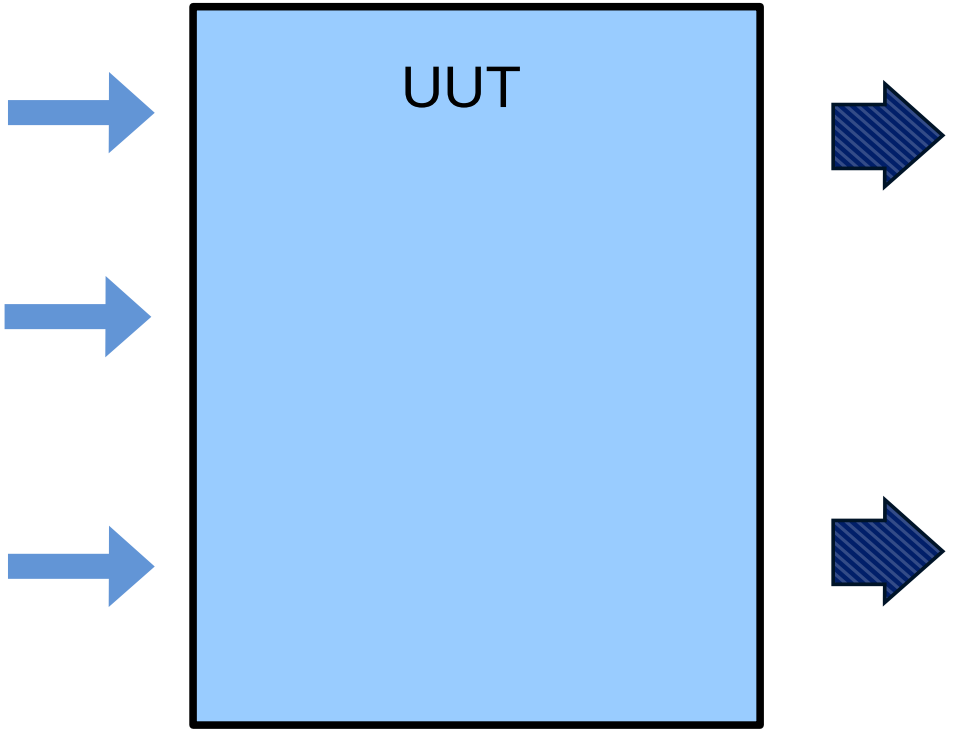
- its inputs can be stimulated and its outputs can be obeserved.

Function Test / FT Type B

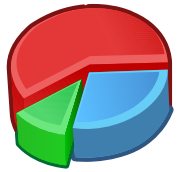
A UUT is regared as testable, if

- it can be set to a known and stable initial state.

- its inputs can be stimulated and its outputs can be obeserved.

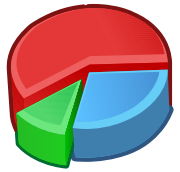


Function Test / FT Type A #1



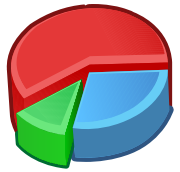
Pros	Cons
Cheap, simple equipment	**- very low** fault coverage - test PASSED does not mean: no faults - fault localisation **cumbersome and time devouring**
Short time required to set up a test procedure	
Adaption to changes of the UUT simple.	Time requirement for test and repair hard to estimate (may get out of hand, operator errors, ...)
simple products: few training required for personell → low labor costs	complex products: highly skilled personell required → high labor costs
system test possible	wrong positioning, orientation, polarity of some parts can **not** be detected (closed case, capacitors). Risk of immediate damages on power-up.

Function Test / FT Type A #2



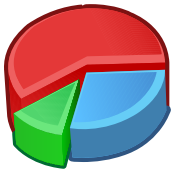
Pros	Cons
Combination with environmental tests possible (reliability, failure rate, ...)	interaction with operator required for für switches, LEDs, displays, buzzer, ...
Periphery can be tested on system level.	**NO clear assertion with regard to quality of solder joints, wiring, ...**

Function Test / FT Type B #1



Pros	Cons
universal automated test equipment (ATE)	moderate test coverage, test PASSED does not mean: no faults
	fault localisation may get cumbersome and time consuming (system level)
automated test procedure → low costs for personell in assembly line	high costs for hardware and test program setup
	low flexibility with regard to changes of the UUT (adaption, wiring, connectors, ...)
	wrong positioning, orientation, polarity of some parts can not always be **detected** (capacitors). Risk of immediate damages on power-up.

Function Test / FT Type B #2



Pros	Cons
combination with environmental tests possible (failure rate, reliability)	interaction with operator required for swiches, LEDs, displays, buzzer, ...
Peripherie kann auf Systemebene getestet werden.	**NO clear assertion with regard to quality of solder joints, wiring, ...**
	capacitive and inductive load due to wiring, cables (EMC)

Function Test / FT Type B #3

Rationale: “*Divide et impera !*“

- Partitions of the UUT are tested as black-box.
- Isolate blocks as small as possible (and reasonable) and test them separately !
  → simplifies test program setup and fault localisation
- If separate blocks are without faults, then the whole system is likely to be faultless too.
- cableforms, wiring → use logarithmic compression

place in the manufacturing process: following structural tests (ICT, FPT, BST)

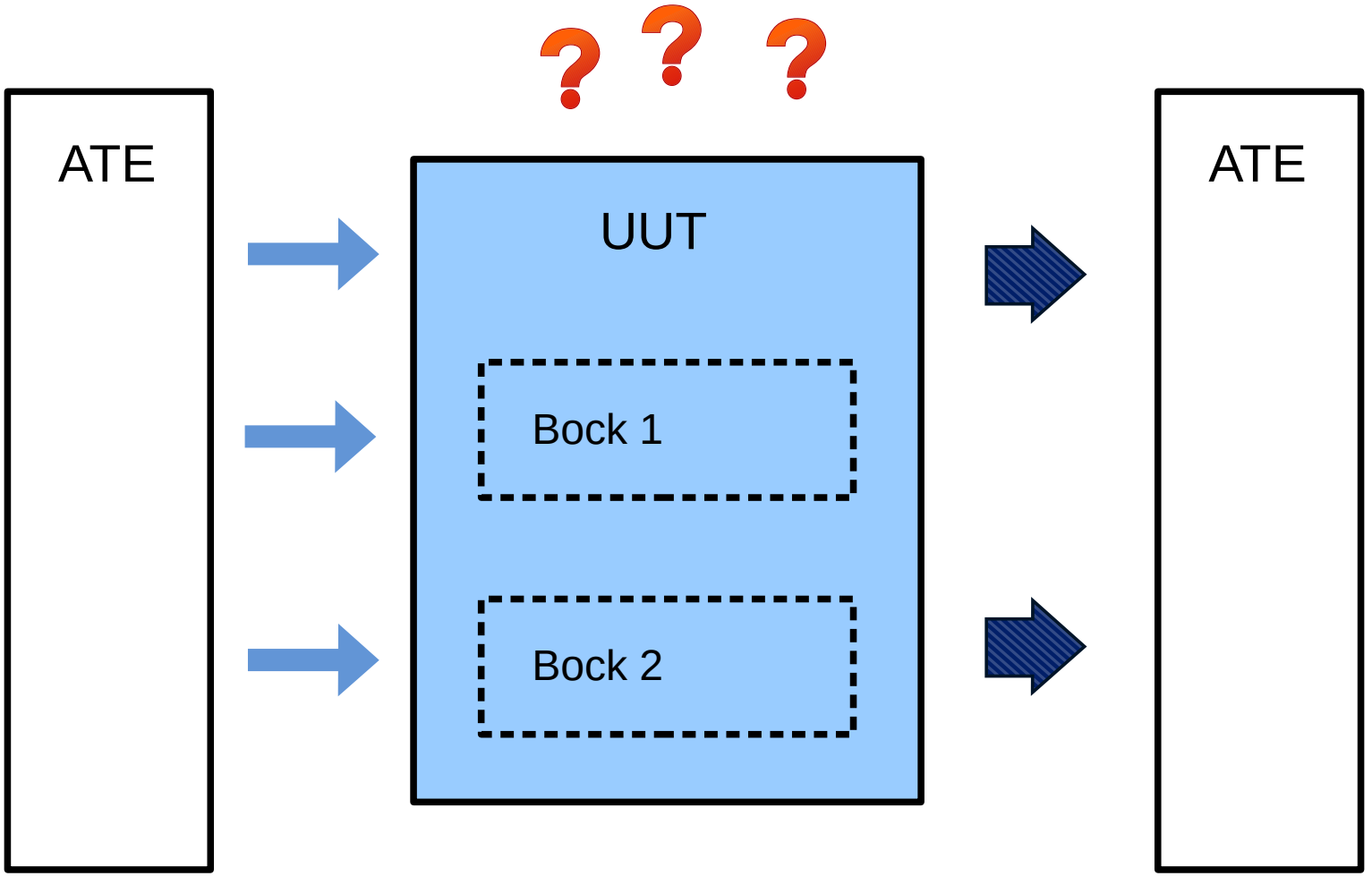
application: single PCBA, device and systemtest

https://www.youtube.com/watch?v=1r4FDyhI9u8

Function Test / FT Type B #4

UUT or partitions are black boxes !

ATE simuliates periphery



Environmentay tests: clima, vibration, dust, ...

Design for Test / DFT #1

A UUT is regared as testable, if

- it can be set to a known and stable initial state.

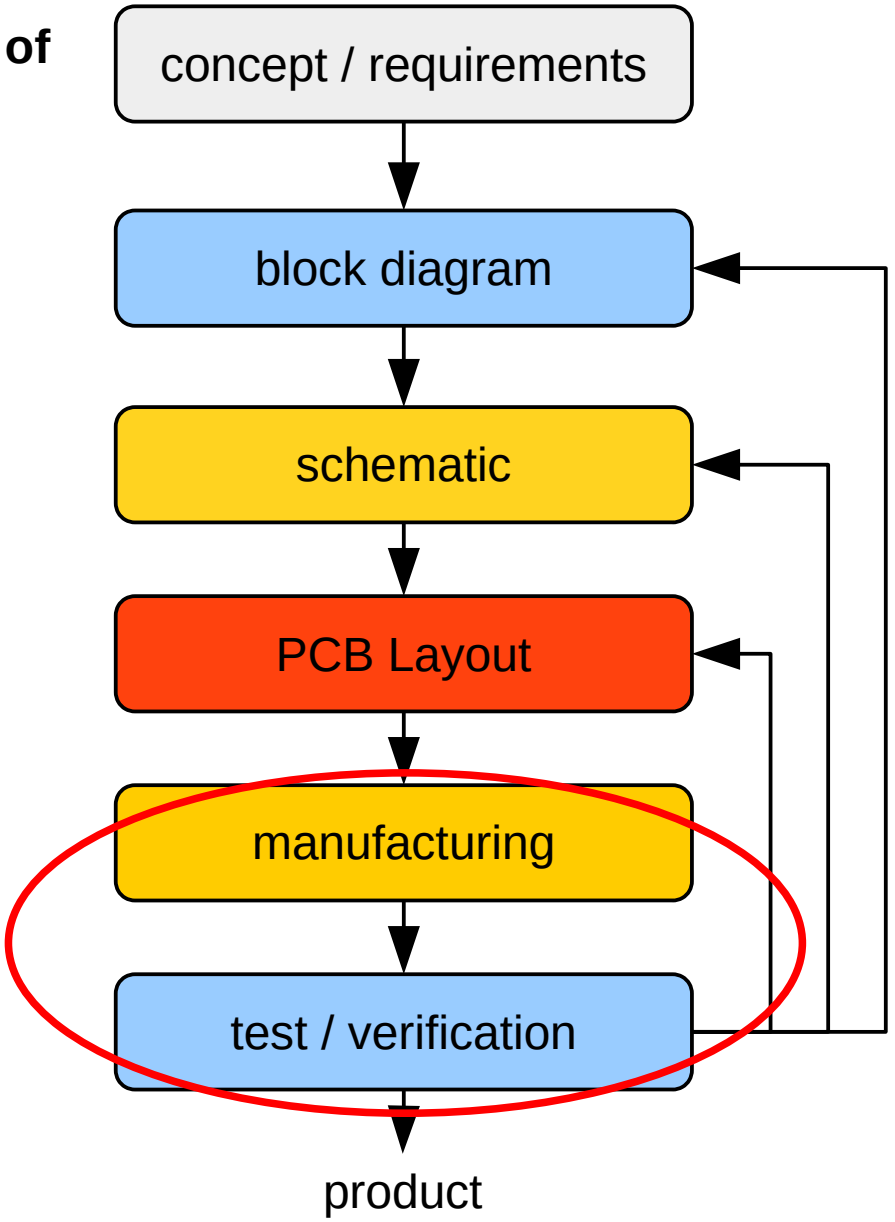
- its inputs can be stimulated and its outputs can be obeserved.

- Problem #1: text compexity increases exponentially with desing complexity
- Problem #2: designers have little knowlede about manufacturing and test (lack of interest, time pressure, ...)
- Problem #3: manufacturing and test staff have litte influence on design and development folks.

We need to talk with each other !

Design for Test / DFT #2

Simplified workflow of HW-engineering:



„other“ construction sites:
- documentation
- logic synthesis
- goods management

Design for Test / DFT #3

- People in design departements need knowledge about processes, tools and methods in manufacturing and test !
- Therefore: → Design For Test !
- „Built-In“ functions that reduce and optimize testing efforts
- DFT reduces time for test development → costs !
- DFT increases test quality → product quality
- DFT applies to ICs, PCBA, devices and systems

Design for Test / DFT #4

Try walking in the shoes of those people who assemble, test, repair, document and sell your design !!!



Design for Test / DFT #5

Basic Rules Part 1

1. Operate parts and components as recommended by the manufacurer.
2. Consider environmenal conditions in the test area (ambient temperature, ...)
3. Testpads/points for In-Circuit-Test (ICT), Flying-Probe-Test (FPT)
4. circuitry for Boundary Scan-test
5. minimize diversity of parts
6. assemble prototypes yourself (use dummy parts)
7. Label parts which require human interaction unambiguously (connectors, LED, trimmers, …)
8. Use unambiguous net names (MCU_RESET_N, MOTOR_ON_OFF, …)
9. Use unambiguous part prefixes (R, C, L, LED, IC, JP, J, X, ...)

Design for Test / DFT #6

Examples for distinct net names:

- PWR_VREG_IN PWR_VREG_OUT PWR_VREG_ADJ
- CPU_JTAG_TCK CPU_JTAG_TMS
- CPU_GPIO_1 CPU_GPIO_2
- P3V3 N12V GND … (*avoid special characters !*)

~~N$0815~~ ~~Öffner_außen_n~~

Design for Test / DFT #7

ANT	ANTENNA
B	BUZZER
BAT	BATTERY
C	CAPACITOR
CA	CAPACITOR_ADJUSTABLE
D	DIODE
DPH	DIODE_PHOTO
DI	DIAC
DIS	DISPLAY
F	FUSE
HS	HEATSINK
IC	INTEGRATED_CIRCUIT
J	JUMPER
JD	JUMPER (for development)
K	RELAY
KP	KEYPAD
L	INDUCTOR
LA	INDUCTOR_ADJUSTABLE
LS	LOUDSPEAKER
LED	LIGHT_EMMITTING_DIODE
LDA	LIGHT_EMMITTING_DIODE_ARRAY
M	MOTOR
MIC	MICROPHONE
N	NETCHANGER
OC	OPTOCOUPLER
Q	QUARTZ
R	RESISTOR
RA	RESISTOR_ADJUSTABLE
RN	RESISTOR_NETWORK
RP	POTENTIOMETER
RPH	RESISTOR_PHOTO
S	SWITCH
T	TRANSISTOR
TP	TRANSISTOR_PHOTO
TF	TRANSFORMER
TPT	TESTPOINT
TH	THYRISTOR
THP	THYRISTOR_PHOTO
TR	TRIAC
TUB	TUBE
X	CONNECTOR
XD	CONNECTOR

Examples IC1, T1, R1, TP1, RN1

Design for Test / DFT #8

m	MILLIOHM
R	OHM
k	KILOOHM
M	MEGAOHM
G	GIGAOHM

p	PICOFARAD
n	NANOFARAD
u	MICROFARAD
m	MILLIFARAD
F	FARAD

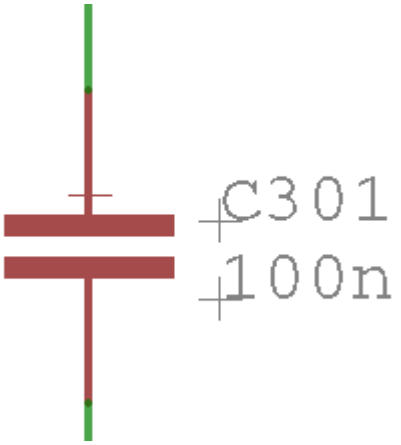
n	NANOHENRY
u	MICROHENRY
m	MILLIHENRY
H	HENRY

V	VOLT
m	MILLIAMPERE
A	AMPERE

k	KILOHERTZ
M	MEGAHERTZ
G	GIGAHERTZ

Examples 4k7, 4n7, 2A5, 3V3

The nature of the part, like resistor, IC, LED, … is clearly visible by the schematic symbol and the prefix:



Avoid special characters: **µ ä ö ü …**
Don’t use space character in the value like: **100 R** !

Design for Test / DFT #9

Basic Rules Part 2 (relevant for ICT / FPT / FT)

- Use vias which are not covered by stop laquer (exceptional cases)
- Make pads of small parts (0201) large enough for nails (ICT, FPT)
- testpads/points for every net (as far as possible and reasonable)
- Finish of pads must be a good conductor (tin, gold, …), mind corrosion.
- size and density of testpads/points (contact manufactuer of nail adaptor)
- Place testpads on bottom side of PCB.
- FPT / ICT: mind angle and dimensions of nails (parts with great height)
- Make sections of a track without stop laquer instead of using a testpad.
- Mind drill sizes of larger vias and THT-pads vs. vacuum-adaptor
- Provide holes to fix the PCBA on an adaptor or test stand.

https://www.electronics-notes.com/articles/test-methods/automatic-automated-test-ate/ict-in-circuit-test-design-for-test-guidelines.php

https://www.embedded.com/design/debug-and-optimization/4430502/Overlooking-design-for-test-can-lead-to-costly-PCB-design-rework

Design for Test / DFT #10

Basic Rules Part 3 (relevant for ICT / FT

- Mind accumulated contact pressure caused by all nails (ICT).
- multi-pole connectors (shrouded pinheaders) can be very sluggish
- reliable galvanic contacts (wear out)
- long livetime of the connectors on the test equipment side
- low ohmic resistance of contacts (sophisticated measurement)
- mind thermovoltages (measurement)
- Feed power supply and GND in parallel via multiple contacts (reduces overall-inductance)
- shielding and twisting of cables and wires (EMC, EMI, SI, ...)

https://www.electronics-notes.com/articles/test-methods/automatic-automated-test-ate/ict-in-circuit-test-design-for-test-guidelines.php

https://www.embedded.com/design/debug-and-optimization/4430502/Overlooking-design-for-test-can-lead-to-costly-PCB-design-rework

Design for Test / DFT #11

Basic Rules Part 4 (relevant for ICT / FPT / BST / FT)

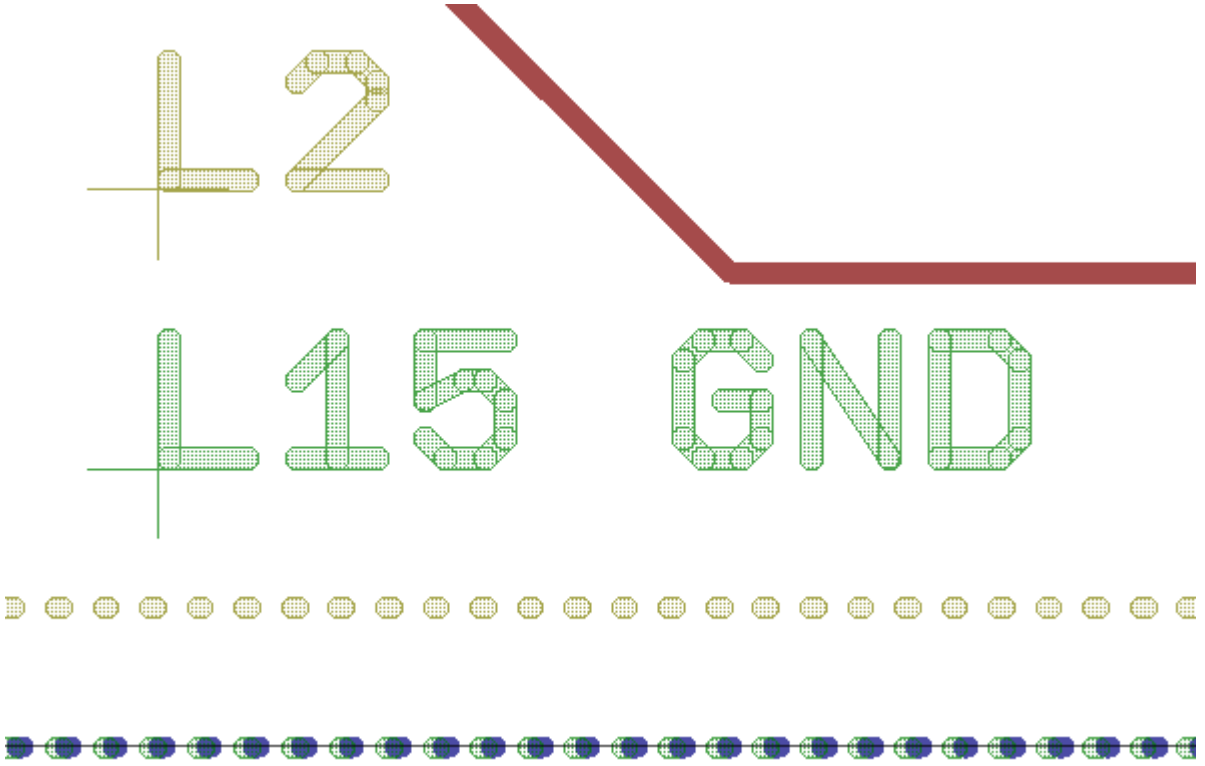
Divide and conquer !

- Separate/isolate small partitions of the circuitry.
- Provide testpads or connectors to control reset- & enable-inputs. Mind pull-resistors !
- Provide means to open feedback loops (amplifiers, control loops, ...)
- Use multiplexers for alternative signal paths (clock)
- Couple-out critical signals (RF) via buffers or impedance converters.
- Extra connectors for test signals (extra costs)
- Mind sequence of power supply voltages on power-up/down.
- Provide means to hook up GND of scope, multimeter, ...
- LEDs for status monitoring
- Inputs may require pull-resistors (unconnected plugs, connectors, ...)

Design for Test / DFT #12

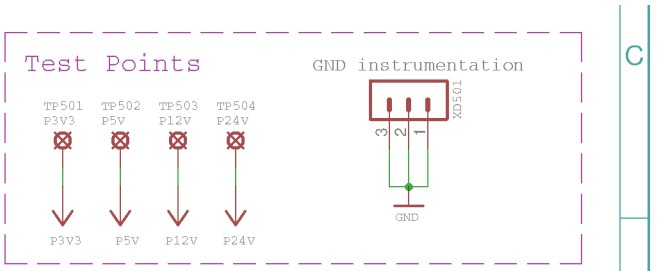
- Texts (even in inner layers) assist design, manufacturing and test (AXI).

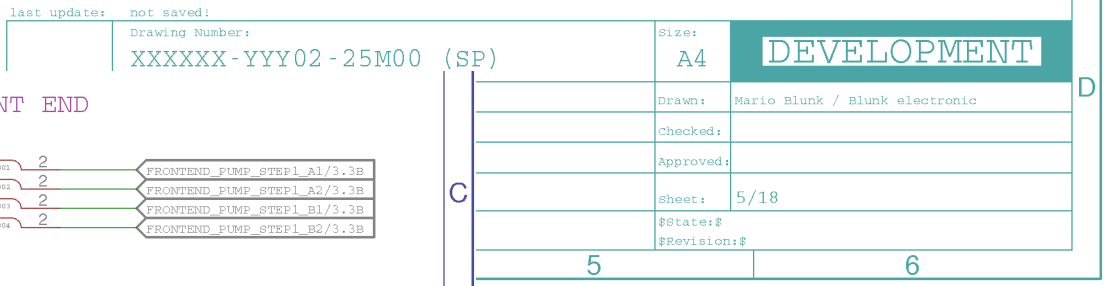
- Mind numbering of signal layers (acc. to IPC top-down) !

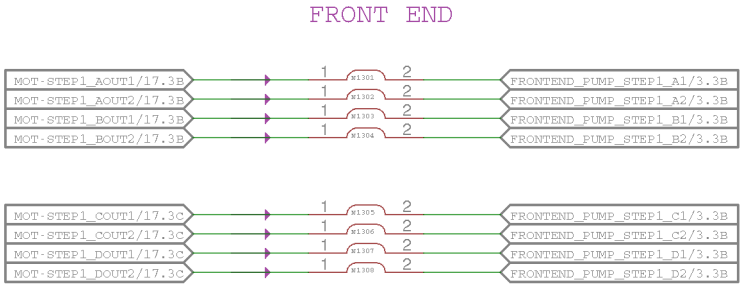


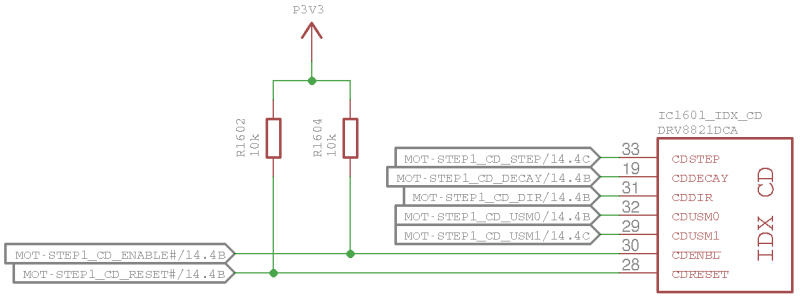
Design for Test / DFT #13

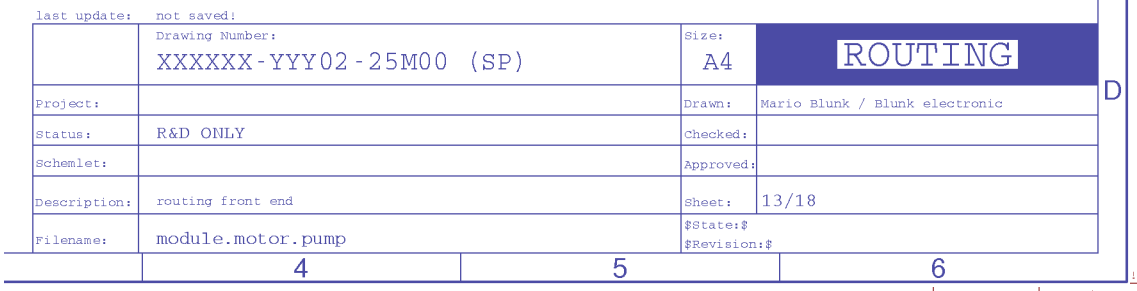
- net names, prefixes, ...
- labeling of schematic sheets
- ISO date format YYYY-MM-DD

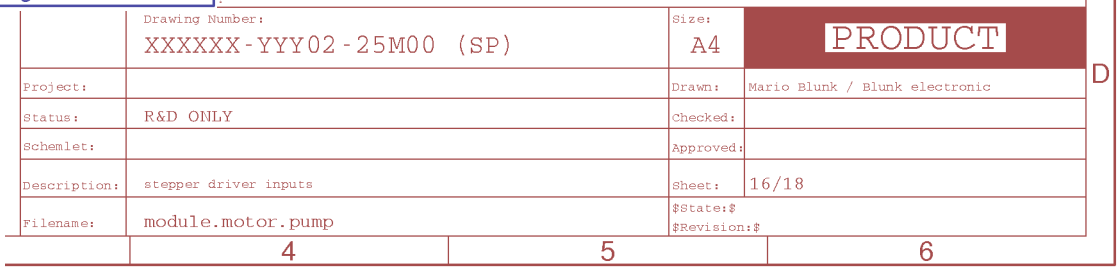




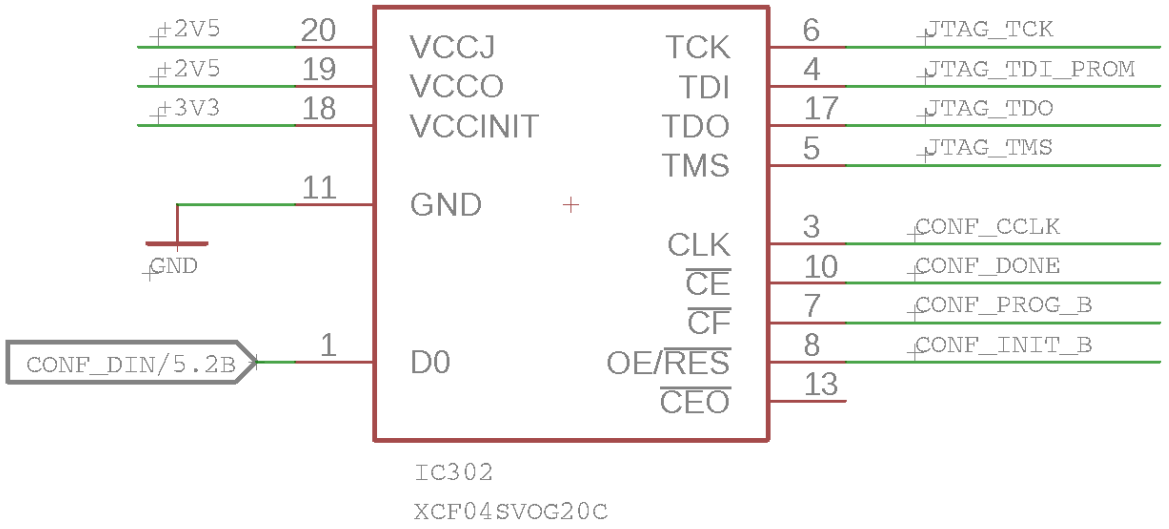


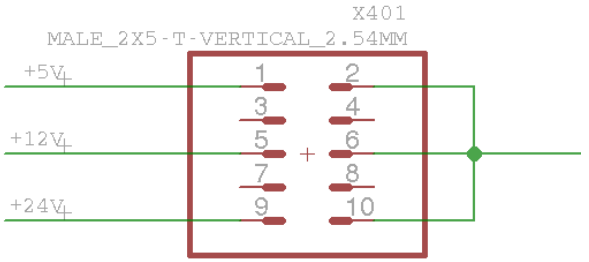




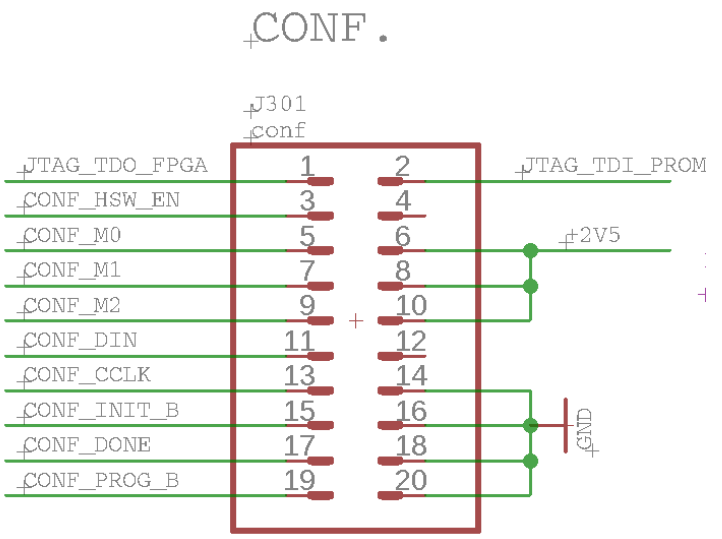


Design for Test / DFT #14



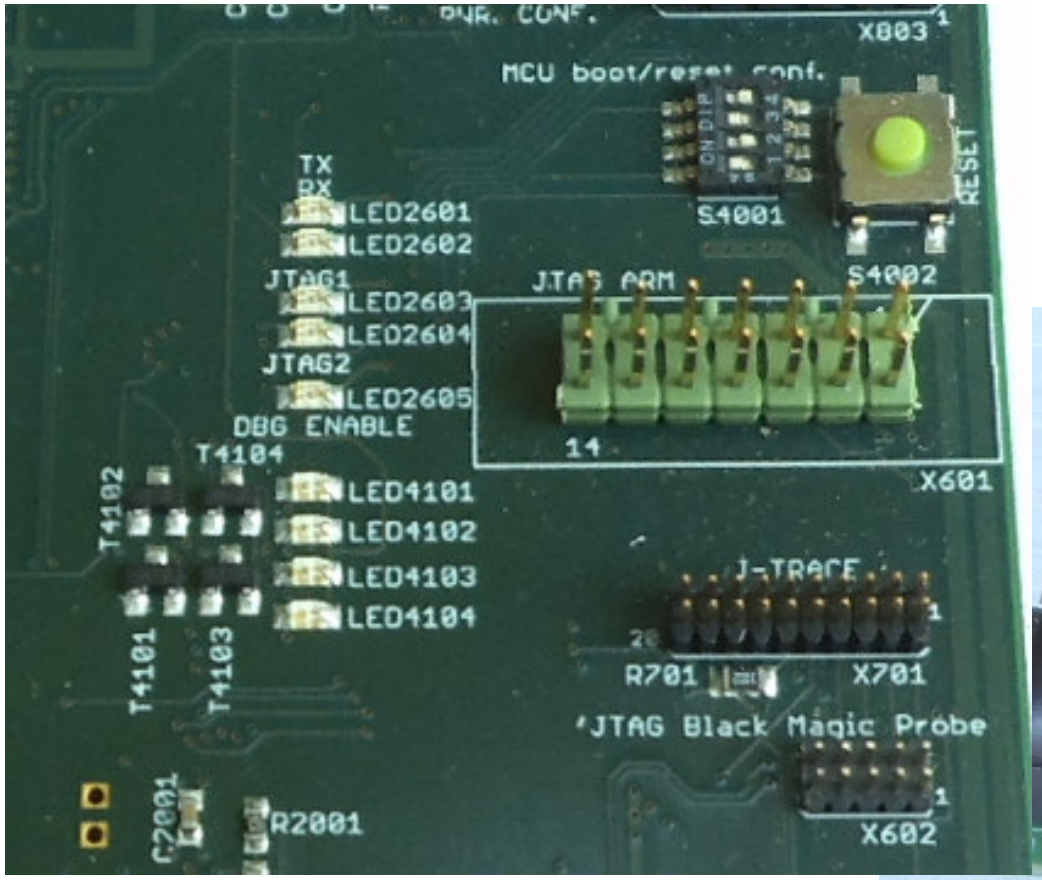


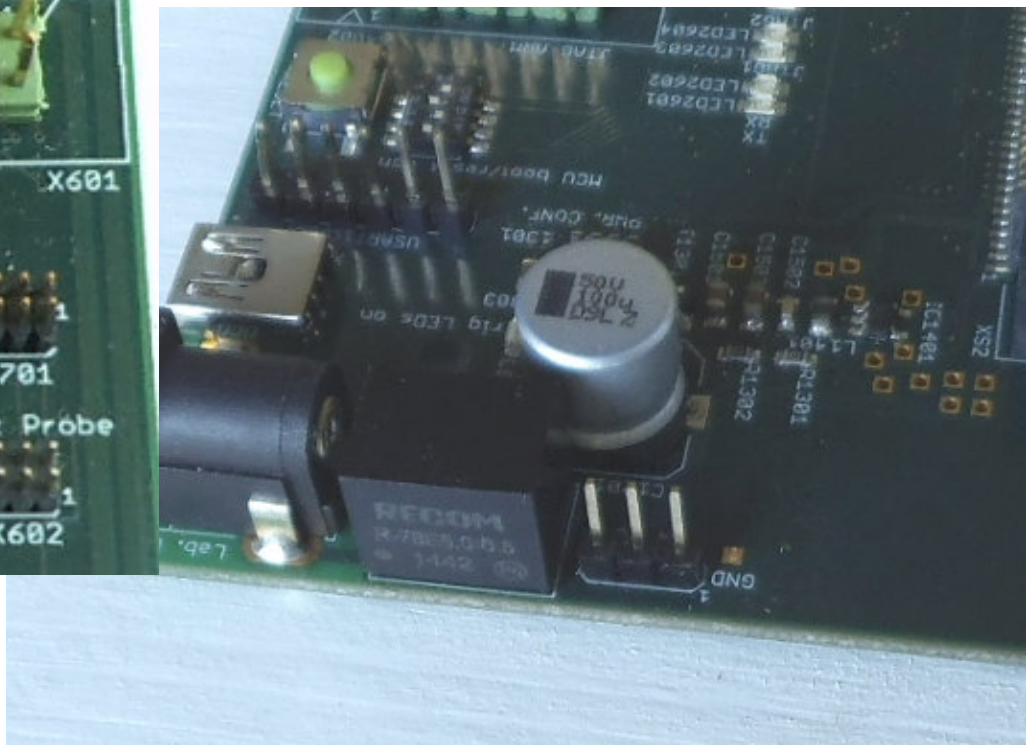
- **avoid Spaghetti !**
- **distribute schematic blocks across sheets**
- **„safe jumpers“**



Design for Test / DFT #15

Hooks, Pinheader, status LEDs, test points, configuration-switches, ...





Design for Test / DFT #16

Basic Rules Part 5 (relevant for BST)

- termination resistors of 300 Ohms each on TCK and TMS to GND on UUT-side (connector)
- optional pull-up-resistors on TDI and TDO
- TRST via jumper, connector or testpoint accessible
- pull-up-resistor on TRST
- SI-conformant layout and wiring between UUT and BS-controller/master
- jumpers to switch to alternative scanpaths via multiplexer or scan-bridges
- jumpers to bypass ICs in the scanpath
- short scanpaths for In-System-Programmierung (ISP)
- WE, OE, CE of PROMs accessible via connector or testpoints
- referencevoltage for BS-controller accessible via connector
- clock of RAMs directly accessible via BS-Treiber (SDRAMs)
- configuration ports of FPGA, CPLD accessible via jumper

Design for Test / DFT #17

Basic Rules Part 6 (relevant for BST)

- Behavior of ports of ICs in test-, normal-, reset-mode may differ !
- pre- and post-configuration BSDL-file required ?
  full galvanic separation of BS-controller and UUT required (integration in ICT/FPT/FT) ?
- Disconnect BS-controller from UUT when UUT is without power.
- Monitor current consumption of the UUT in test mode (Debugger !)
- Feed power supply and GND in parallel via connectors (reduces the overall-inductance of the wires)

Literature References

[Kärger, 85] Kärger, Reinhard: German „Prüftechnik für elektronische Erzeugnisse“
1985 Verlag Technik Berlin

[Kärger, 96] Kärger, Reinhard: German „Diagnose von Computern“
1986 Verlag B. G. Teubner Stuttart

[IEEE1149] The Institute of Electrical and Electronics Engineers, Inc. , 3 Park Avenue,
New York, NY 100165997, USA; IEEE Std 1149.12001
“IEEE Standard Test Access Port and Boundary Scan Architecture”

[Parker, 15] Parker, Kenneth: „The Boundary-Scan Handbook“
Springer Verlag

http://www.blunk-electronic.de/bsm/Boundary_Scan_Basics.pdf

http://www.blunk-electronic.de/bsm/how_to_test.pdf

http://www.blunk-electronic.de/bsm/System_M-1_Manual_en.pdf

https://pdfs.semanticscholar.org/ba9a/aeda85a6b3a1ac966b950b36c7078c54f645.pdf

http://www.smtnet.com/library/files/upload/DFT%20and%20Inspection.pdf

http://www.blunk-electronic.de/pdf/Design_Checklist_en.pdf

https://www.electronics-notes.com/articles/test-methods/automatic-automated-test-ate/ict-in-circuit-test-design-for-test-guidelines.php

https://www.embedded.com/design/debug-and-optimization/4430502/Overlooking-design-for-test-can-lead-to-costly-PCB-design-rework

Thank you for your attention !