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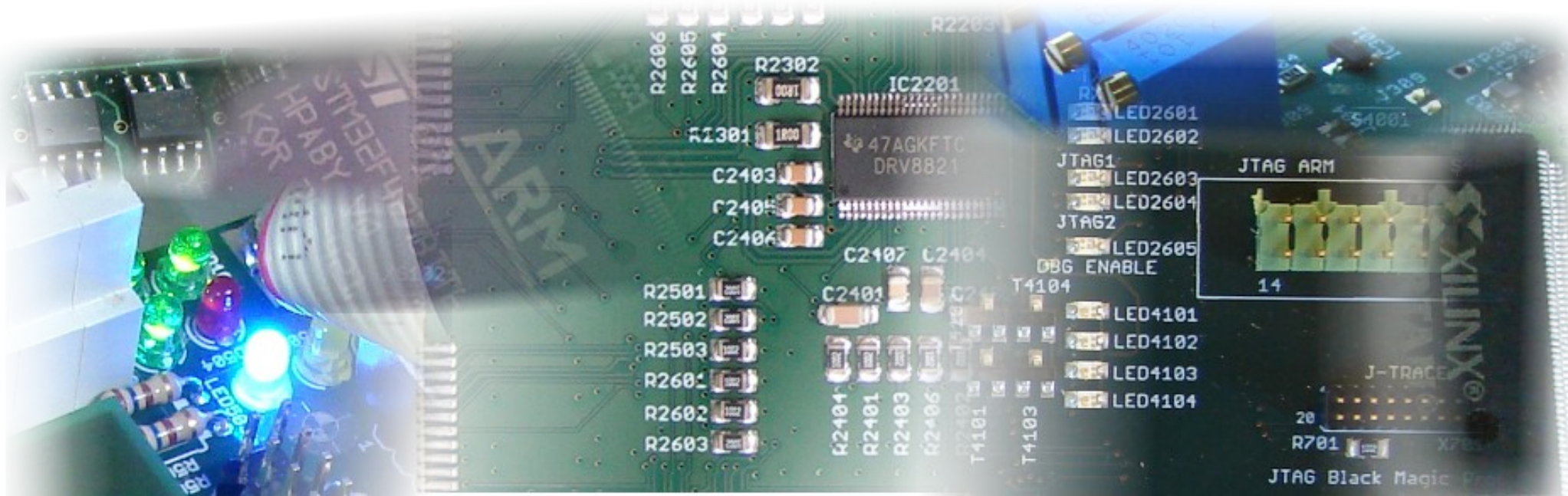
Email info@blunk-electronic.de

Internet www.blunk-electronic.de



Design Reviews Gutachten Beratung

HW/SW-Entwicklung Boundary Scan / IEEE 1149.x



Agenda

Modul 1

Tag #1

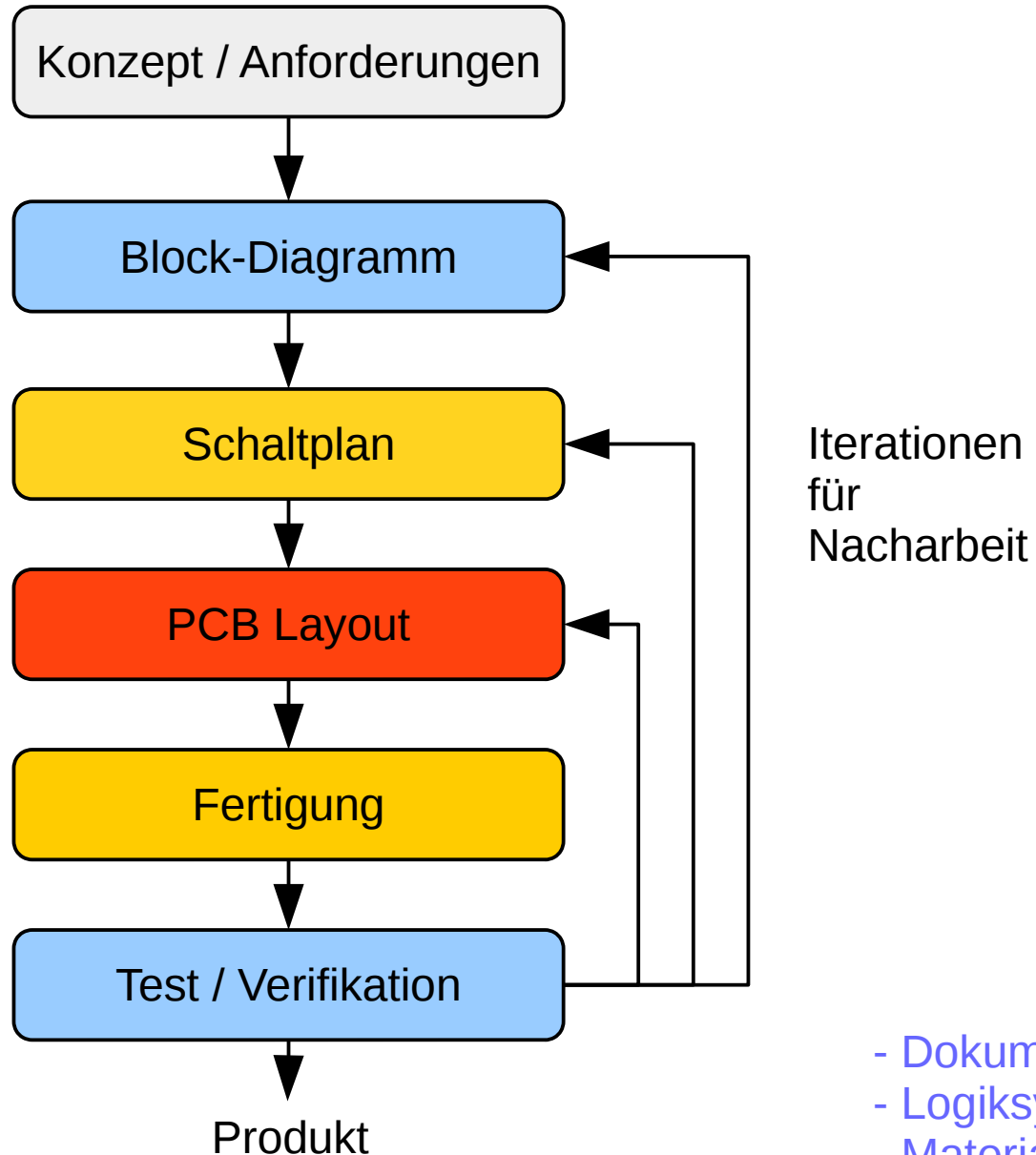
- Überblick HW-Entwicklung
- Schaltplan erstellen
- Dokumentation
- Netzklassen festlegen
- Electrical Rule Check (ERC)
- Vorbereitung PCB-Layout
- Konturen Leiterplatte
- Paßmarken, Bohrungen

Tag #2

- Platzierung Bauteile
- Bestückungsdruck
- Design Rules (DRC)
- Lagenaufbau, Via-Typen
- Routing / Entflechtung
- Bauteile in Bibliothek bearbeiten/anlegen
- CAM-Prozessor

HW-Entwicklung

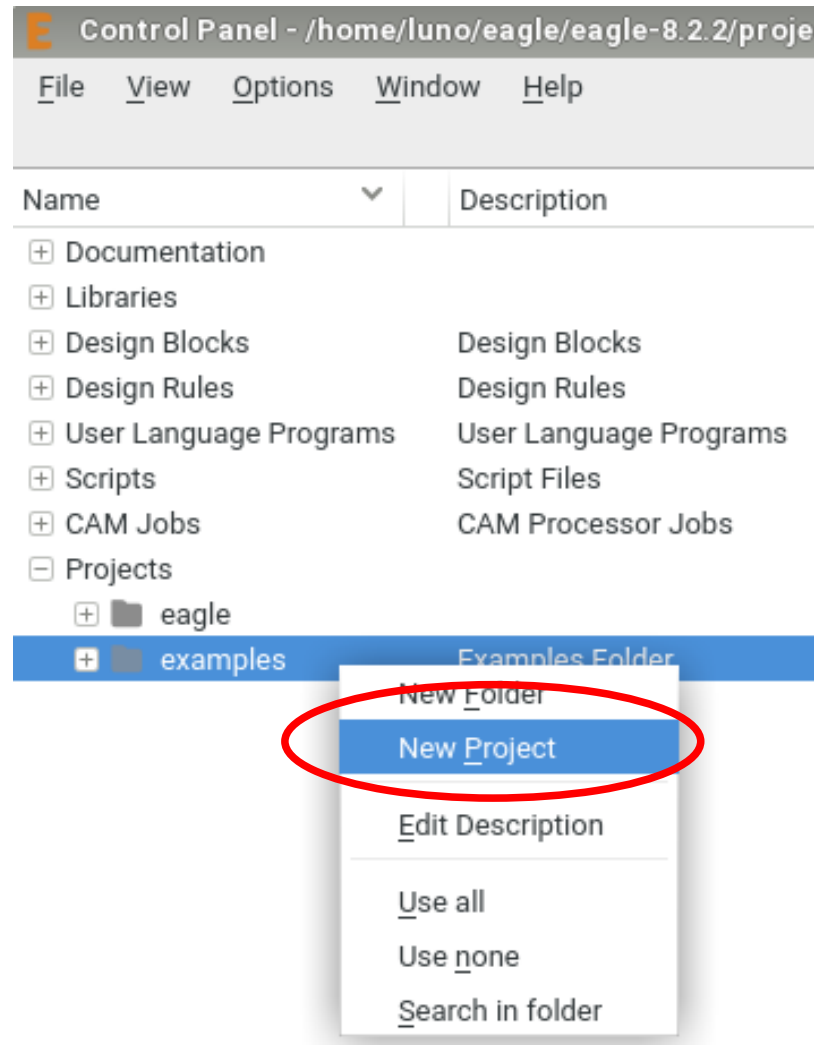
vereinfachter Ablauf:



- Dokumentation
- Logiksynthese
- Materialwirtschaft

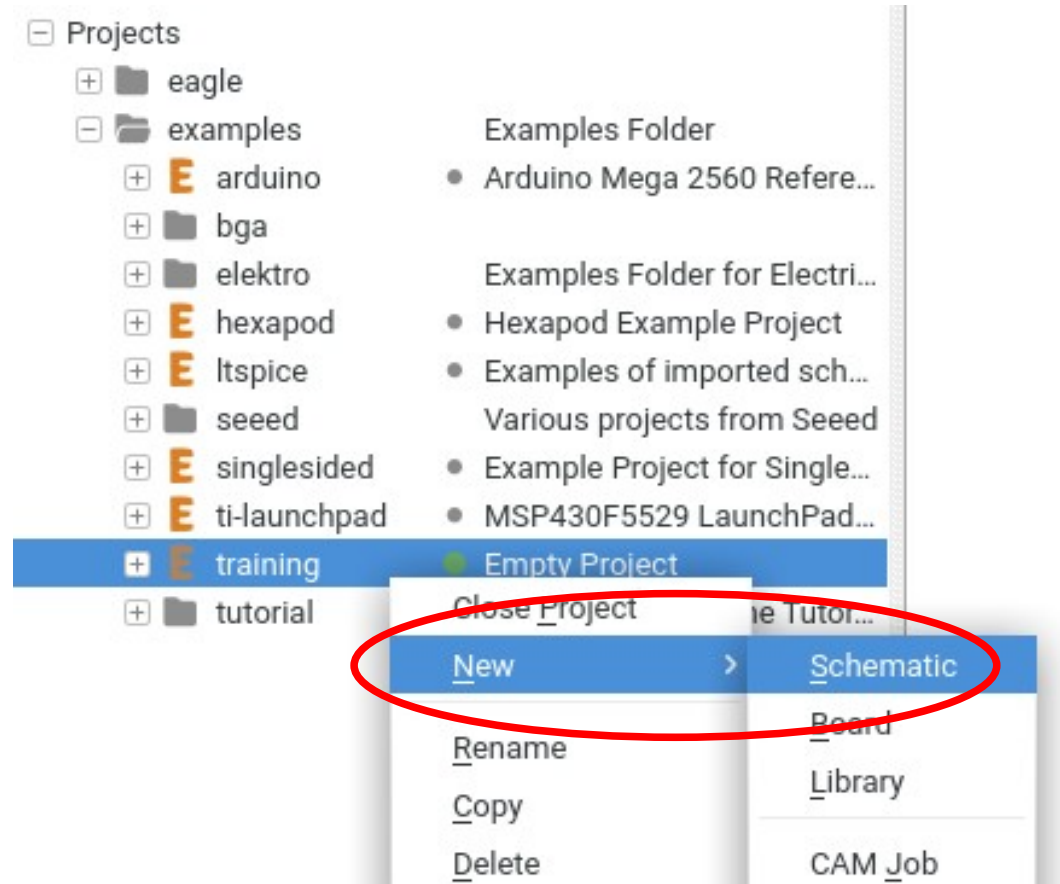
Anlegen des Projektes

Rechtsklick /
Neues Projekt

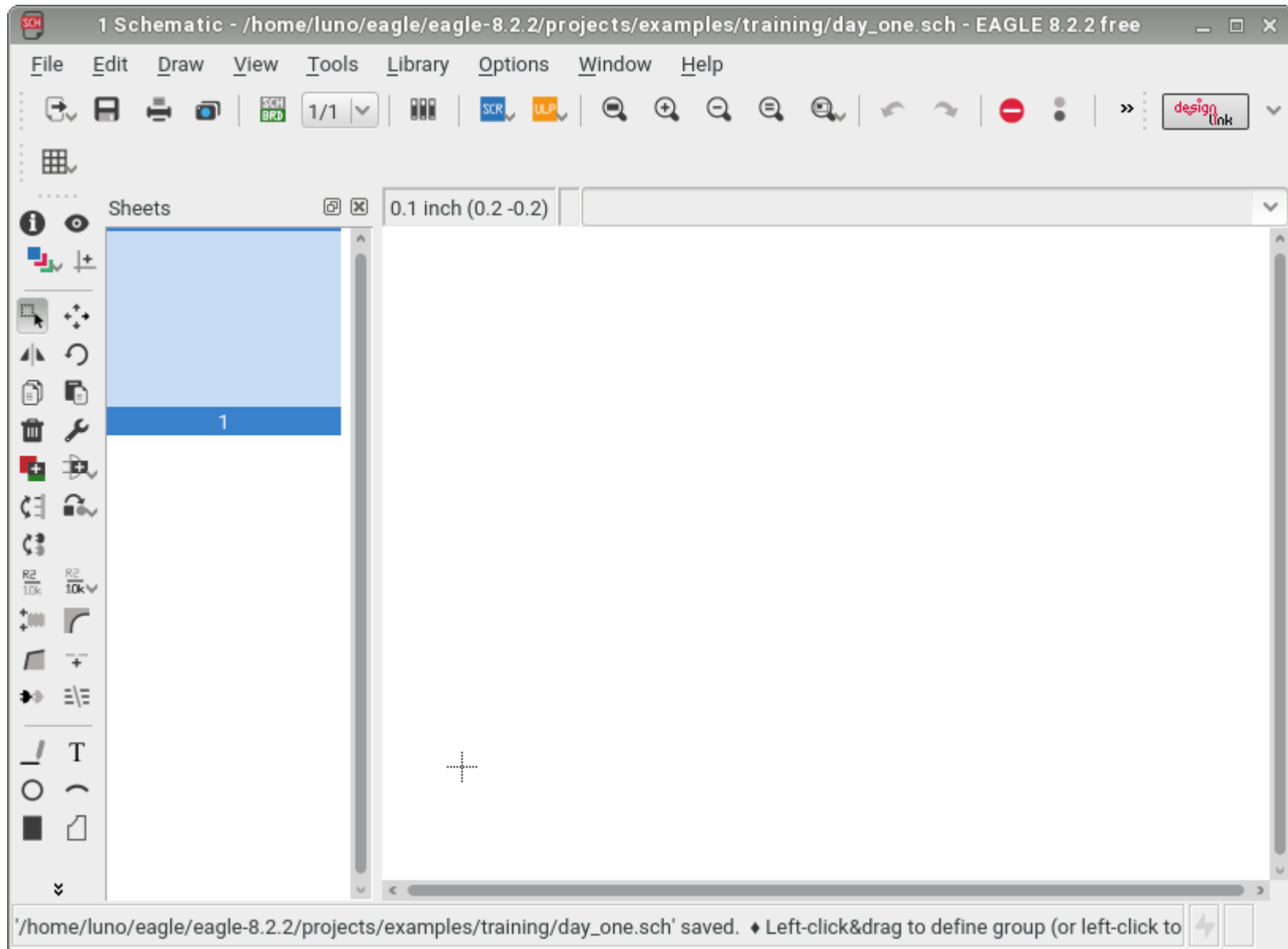


Schaltplan anlegen #1

Rechtsklick auf
Projektname /
Neuer
Schaltplan

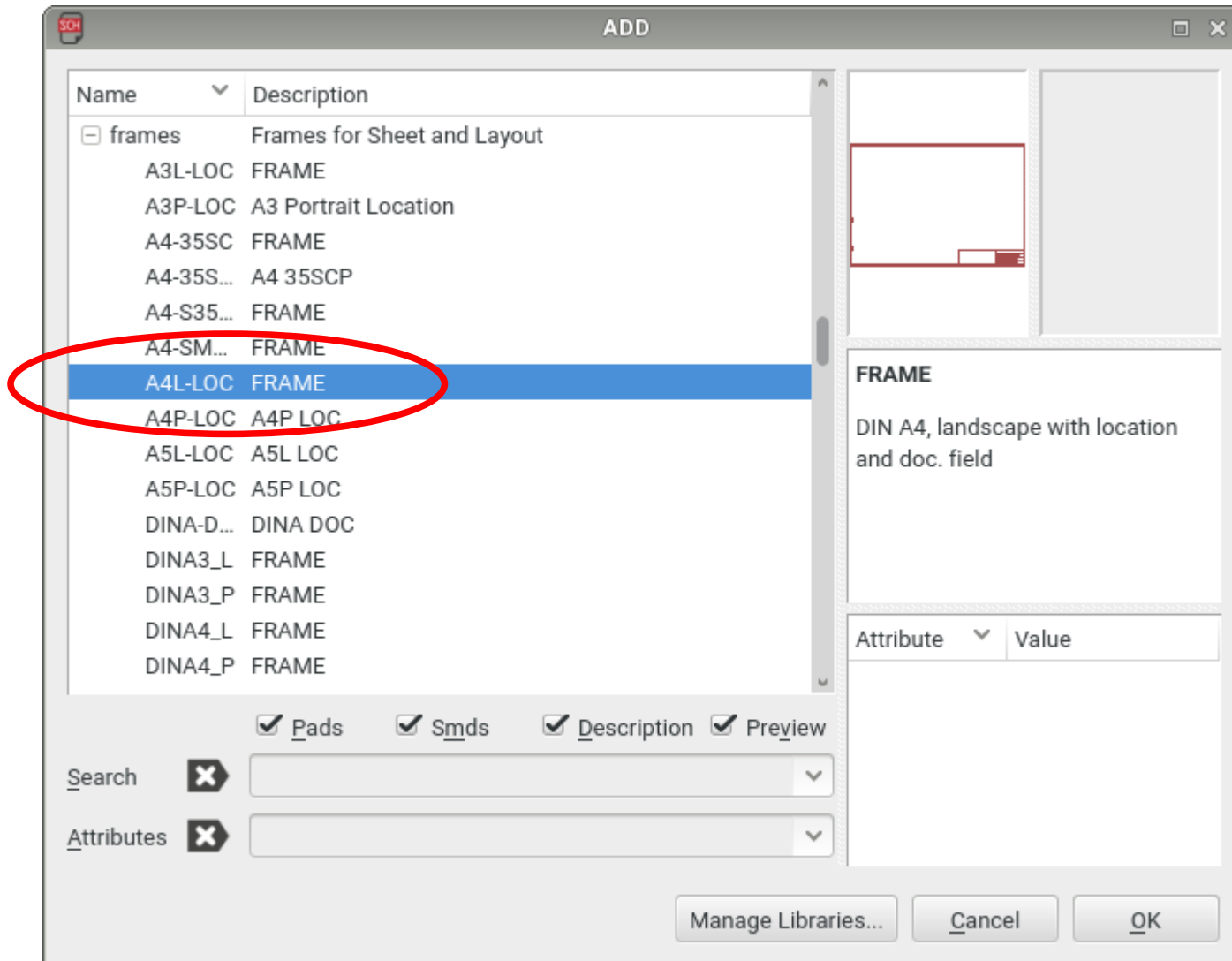


Schaltplan anlegen #2



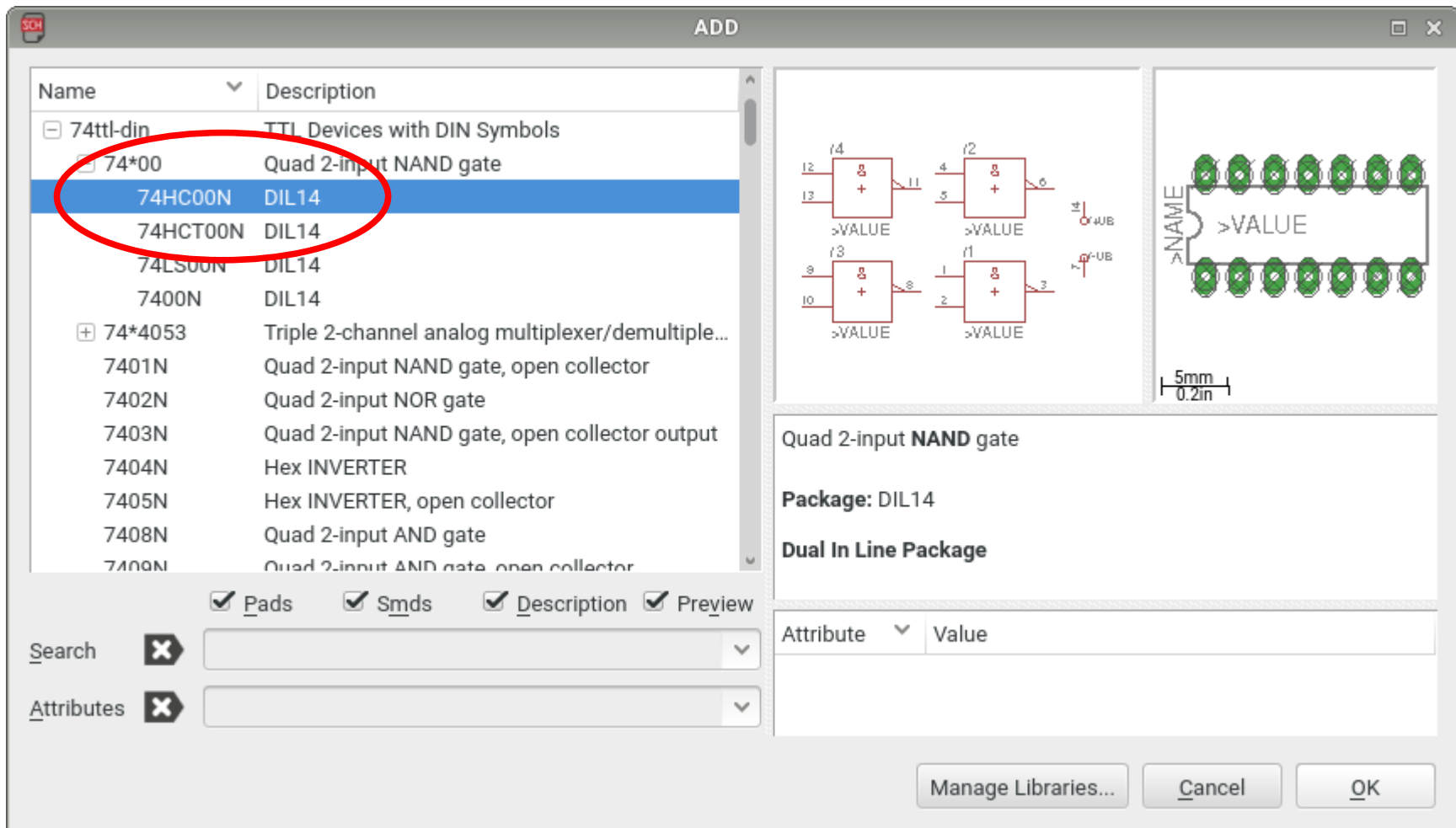
Zeichnungsrahmen

Befehl ADD



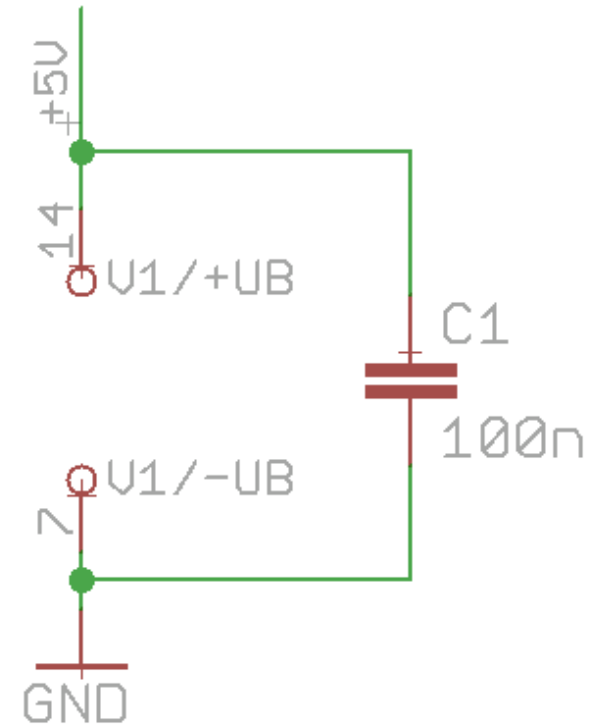
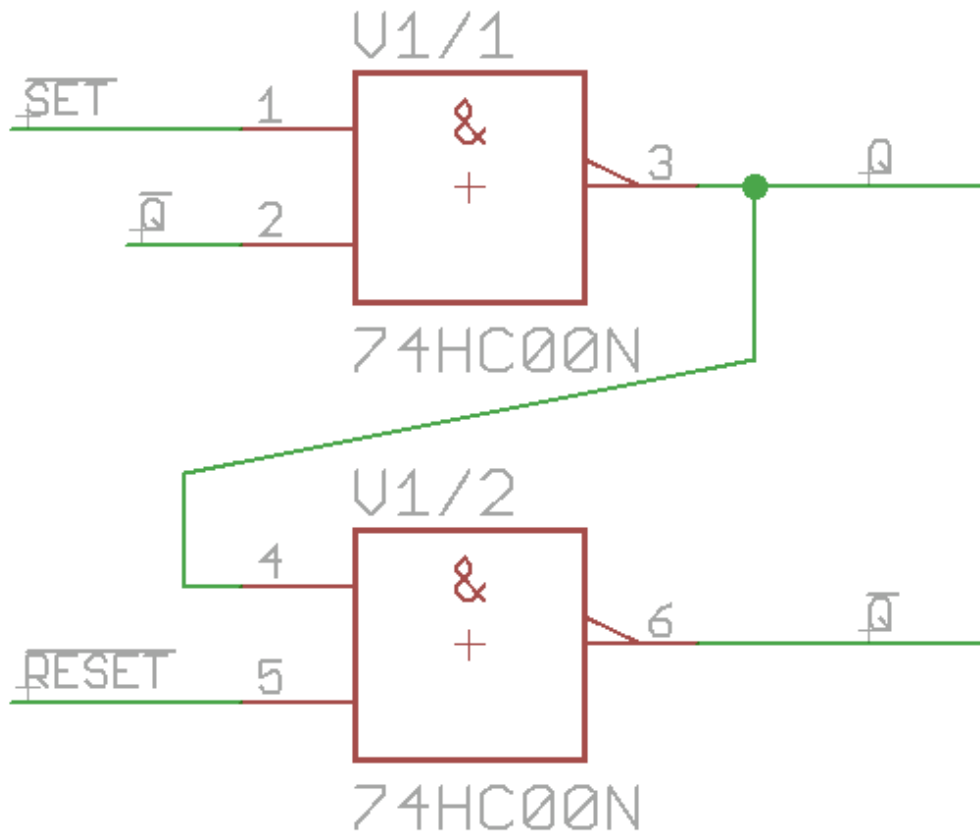
Bauteile platzieren #1

Befehle **ADD**, **USE**, **MOVE**, **DELETE**, **GROUP**,
NAME, **VALUE**, **CHANGE**, **SMASH**



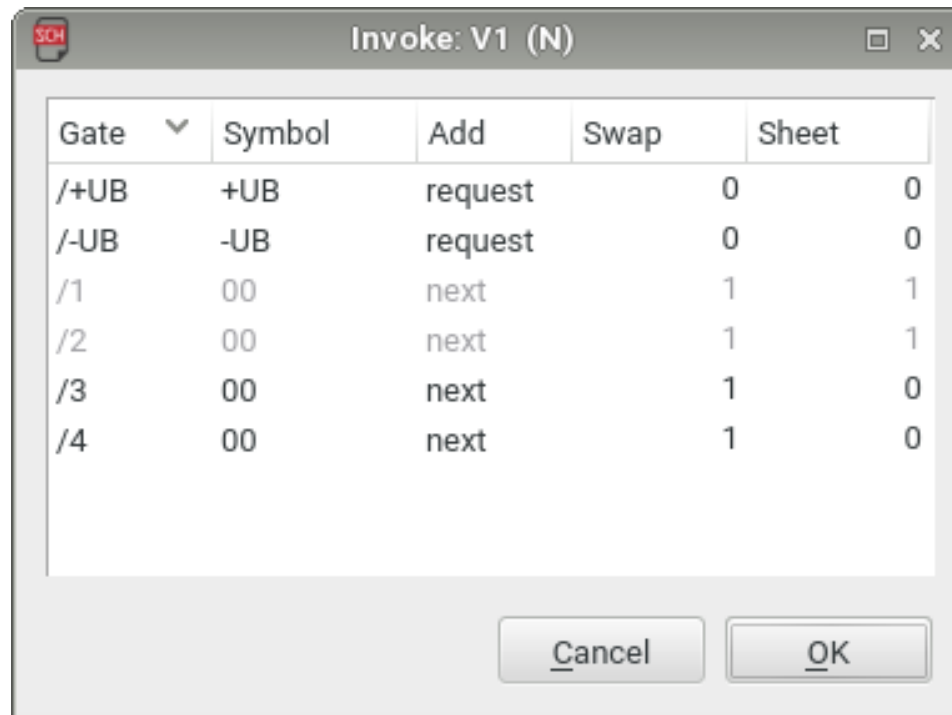
Bauteile platzieren #2

Befehle NET, NAME, LABEL, SPLIT,
JUNCTION, SHOW



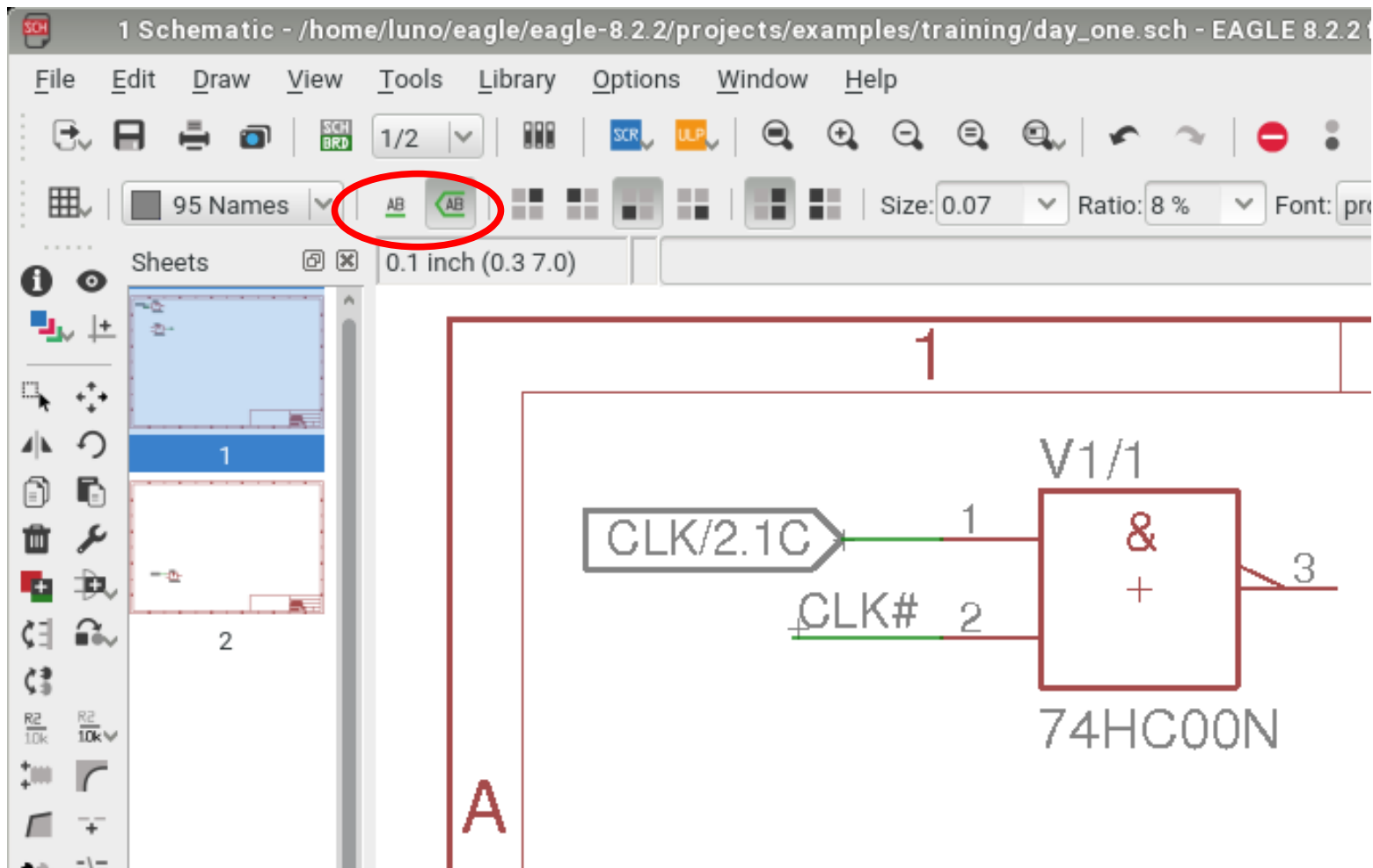
Bauteile platzieren #3

Befehl **INVOKE** oder seitenübergreifend
INVOKE V1



Netze

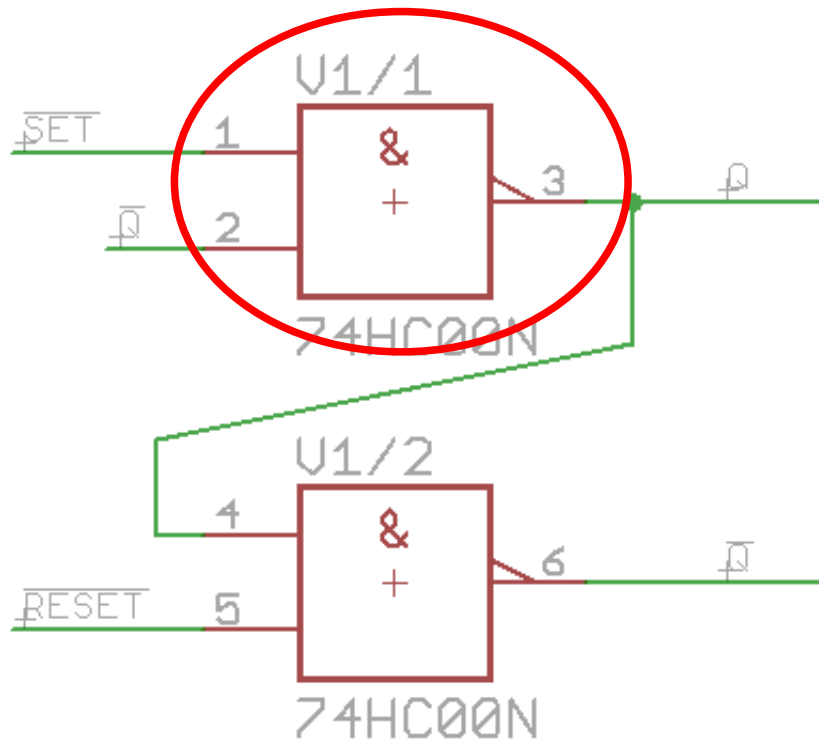
Befehle LABEL, MOVE, DELETE



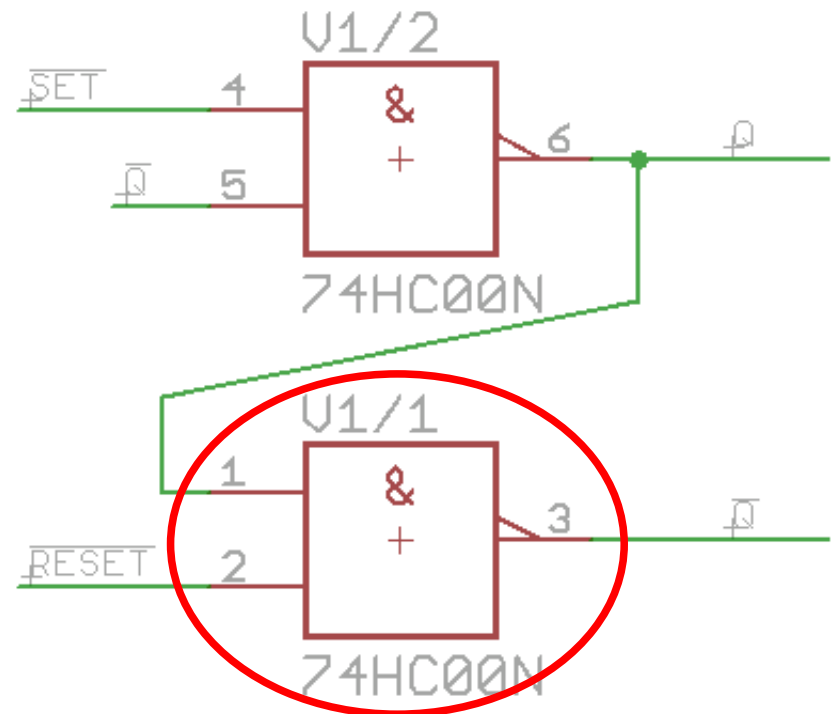
Gate Swap

Befehl **GATESWAP**

vorher

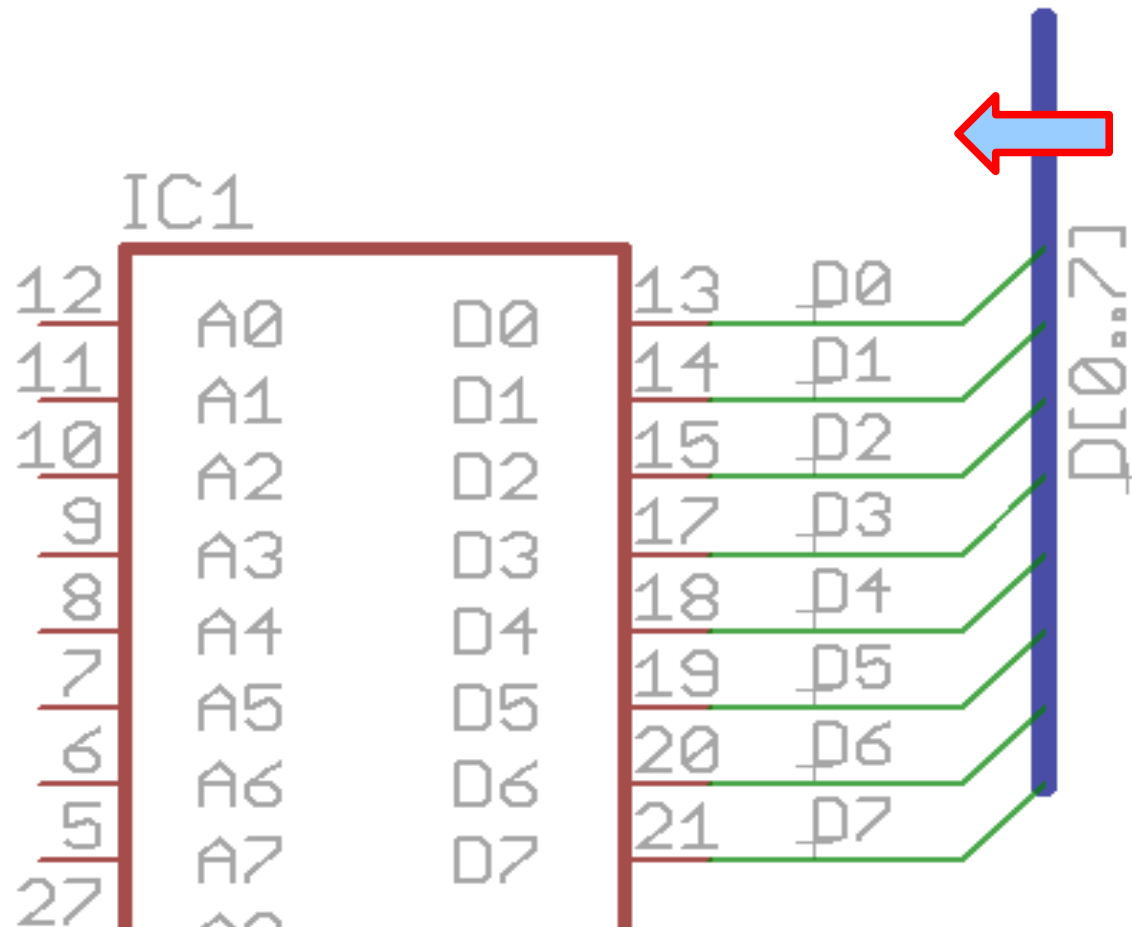


nachher



Busse

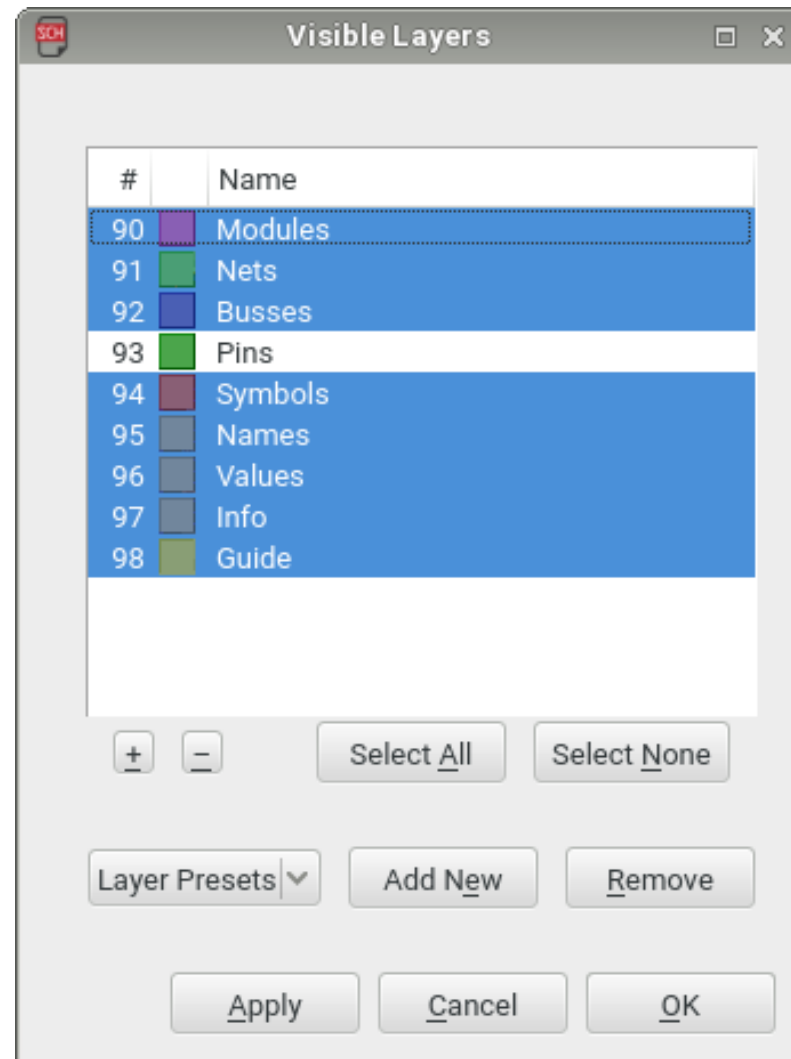
Befehle **BUS**, **NAME**, **LABEL**, **SPLIT**



Schaltplan Layer

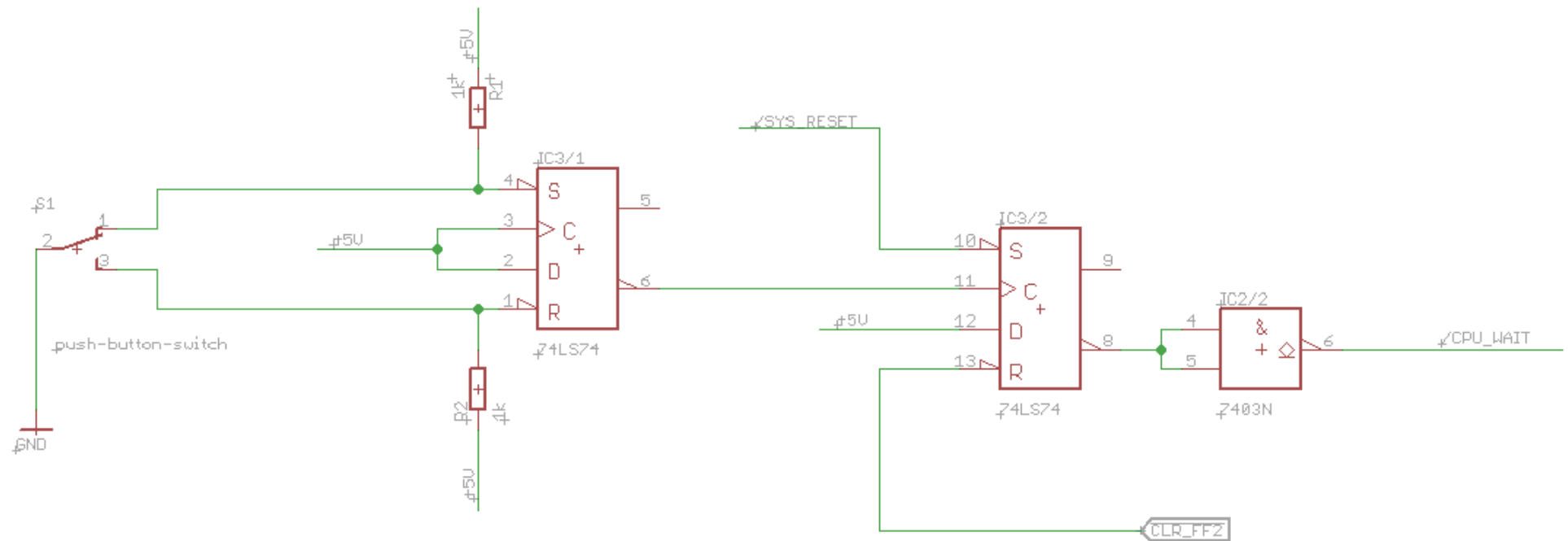
Befehle

**DISPLAY,
LAYER,
CHANGE LAYER**

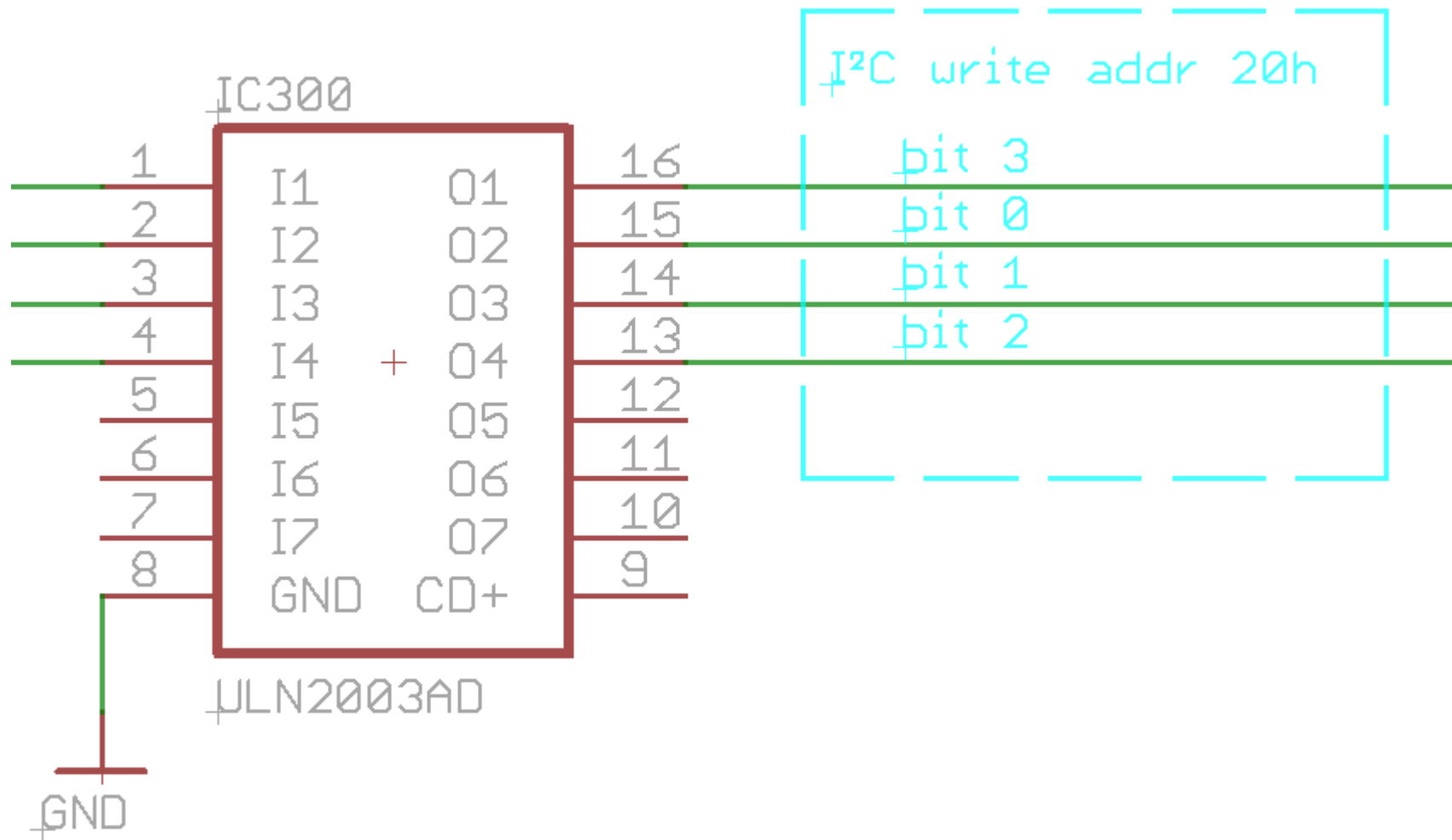


Dokumentation #1

Cycle Stepper



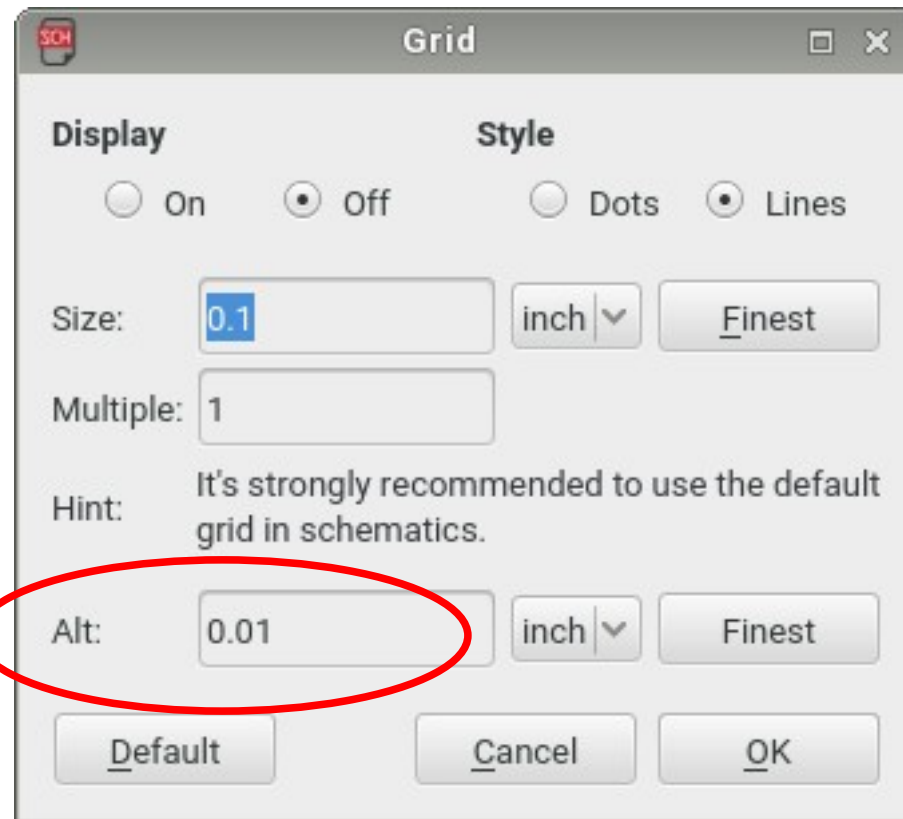
Dokumentation #2



Zeichnungsraster



Befehl **GRID**



Alternativ Grid:

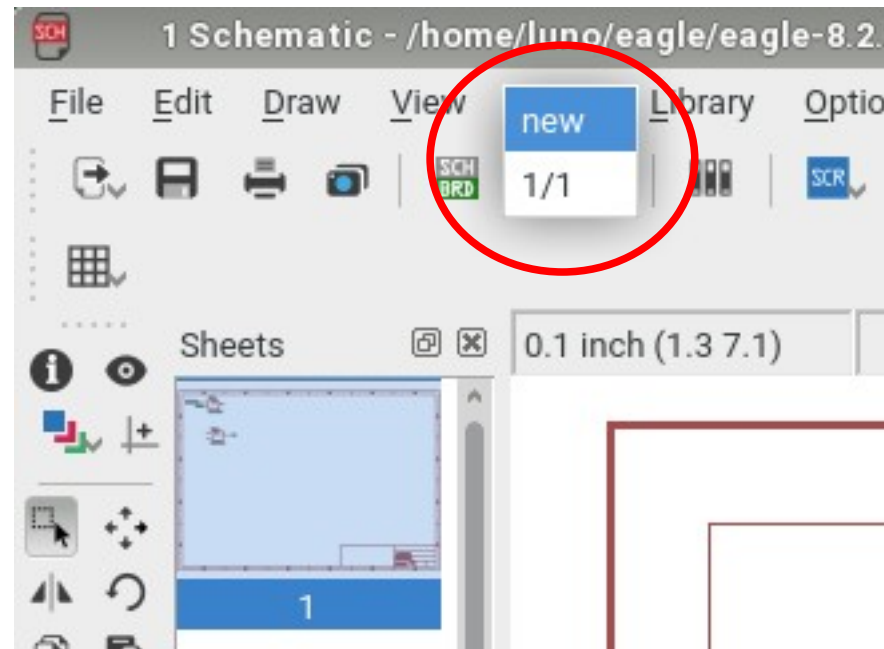


Strg+Alt

Schaltplan - Seiten

Befehl **EDIT .s2**

Sortieren mit
EDIT .s2 .s1



Netzklassen #1

regeln Minimalwerte :

Bahnbreite **Via-Bohrungen** **Abstand zu anderen Signalen**

Befehl
CLASS

Nr	Name	Width	Drill	Clearance
<input checked="" type="radio"/> 0	default	10mil	0mil	10mil
<input type="radio"/> 1	PWR	40mil	0mil	20mil
<input type="radio"/> 2	GND	50mil	0mil	20mil
<input type="radio"/> 3		0mil	0mil	0mil
<input type="radio"/> 4		0mil	0mil	0mil
<input type="radio"/> 5		0mil	0mil	0mil
<input type="radio"/> 6		0mil	0mil	0mil
<input type="radio"/> 7		0mil	0mil	0mil

Netzklassen #2

Befehle

INFO,

CHANGE CLASS

Properties

Wire

From 1 6.6

To 0.8 6.6

Length 0.2

Angle 180

Width 0.006

Style continuous

Curve 0

Net

Name CLK

Net Class 0 default

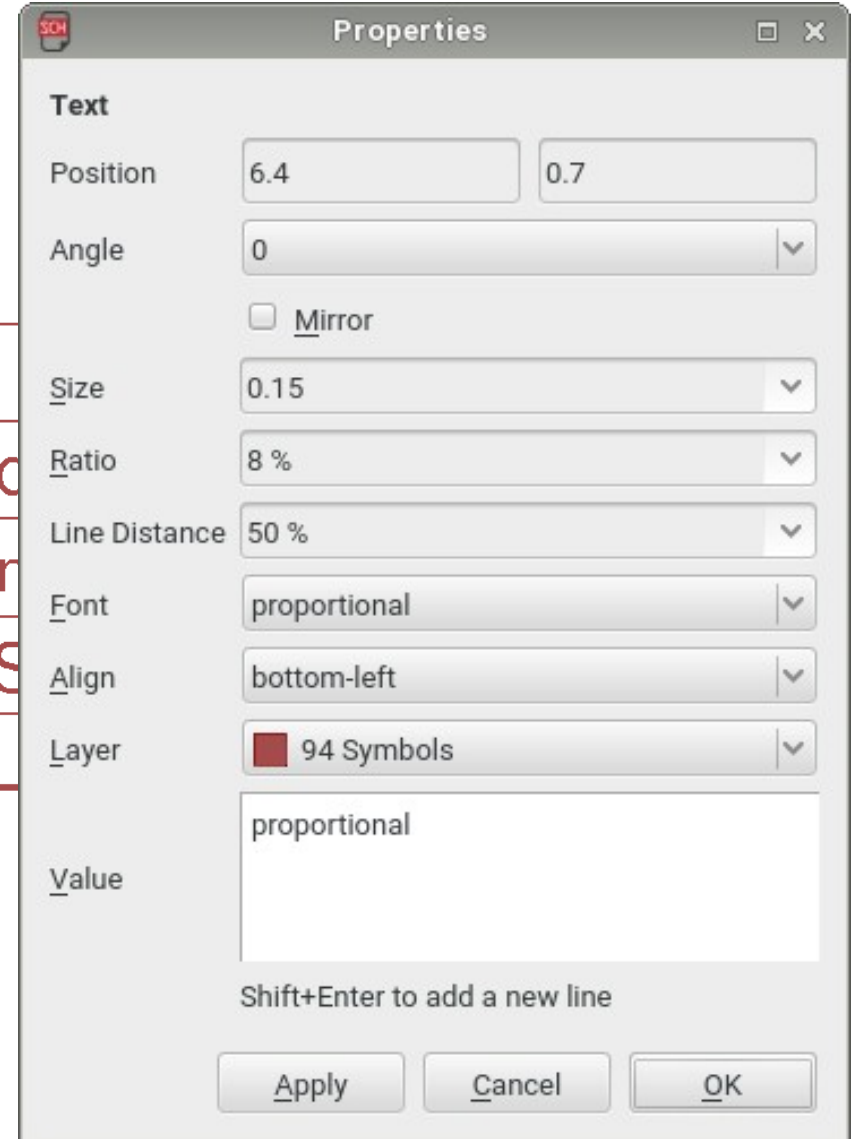
Allocation

Sheet	Row	Column
1	A	1

Apply Cancel OK

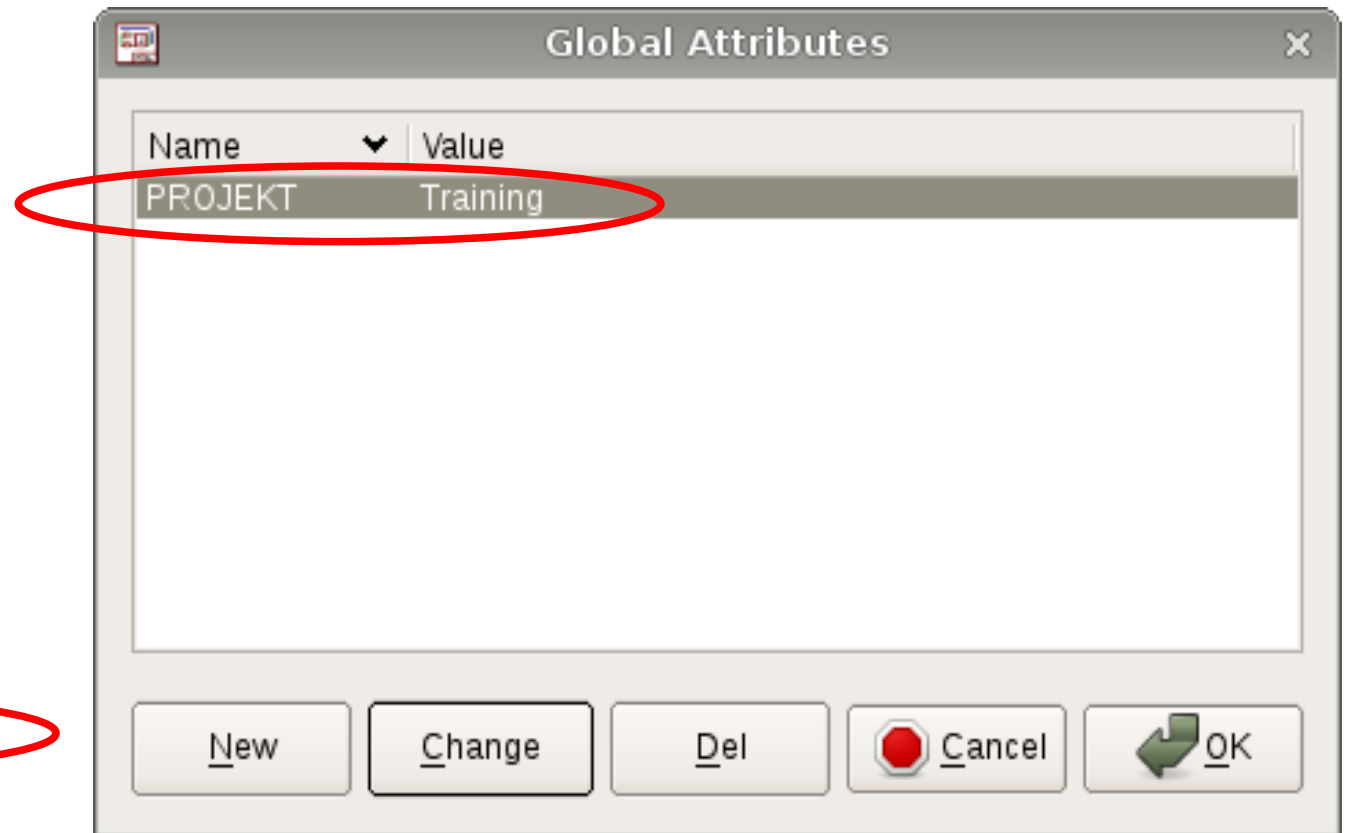
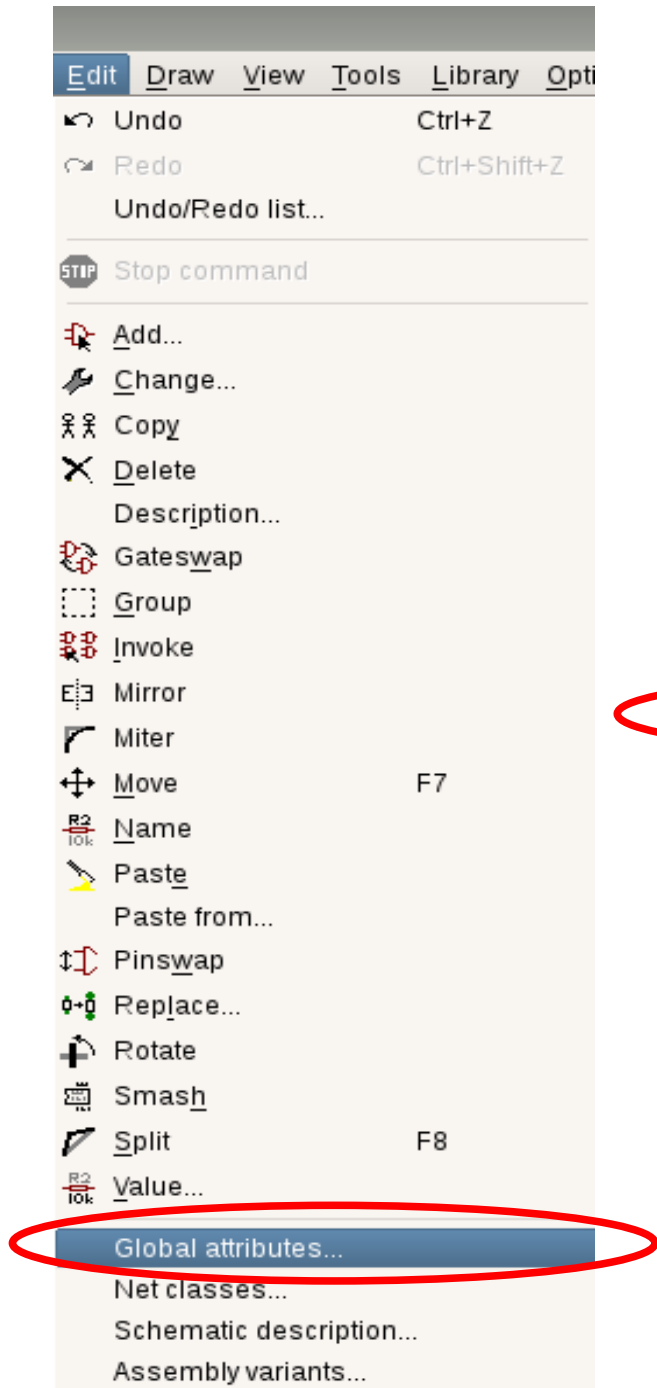
Texte #1

Befehle **TEXT**, **INFO**

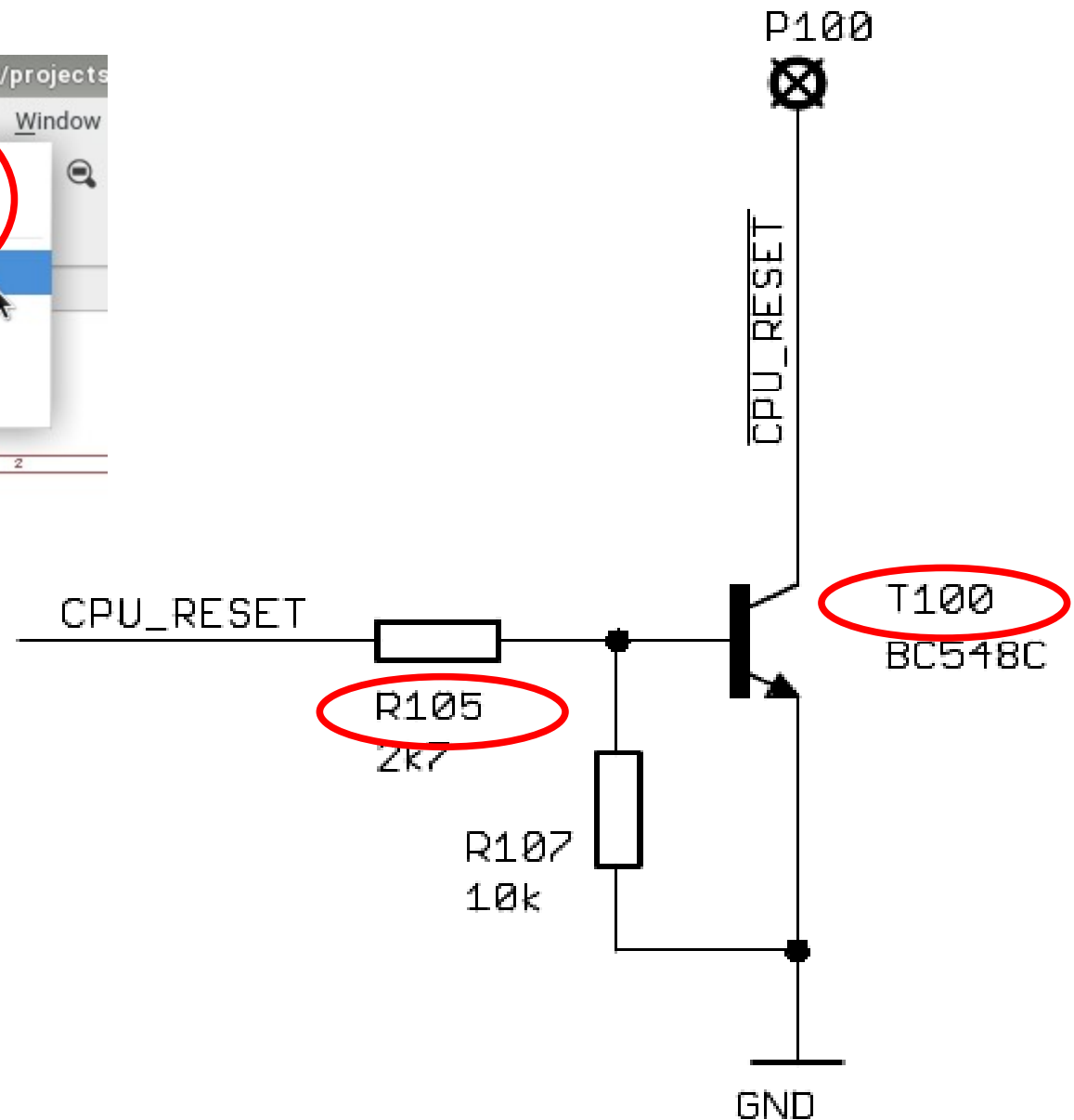
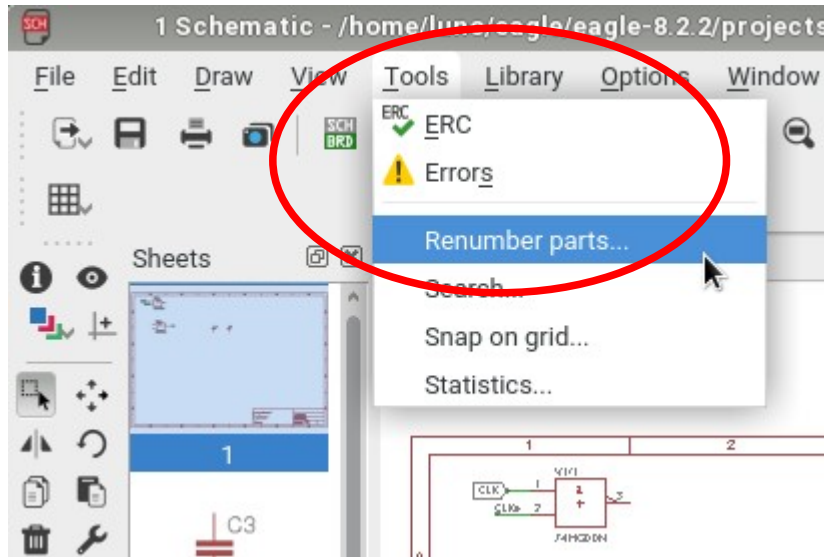


Texte #2

Befehl **TEXT** > PROJEKT

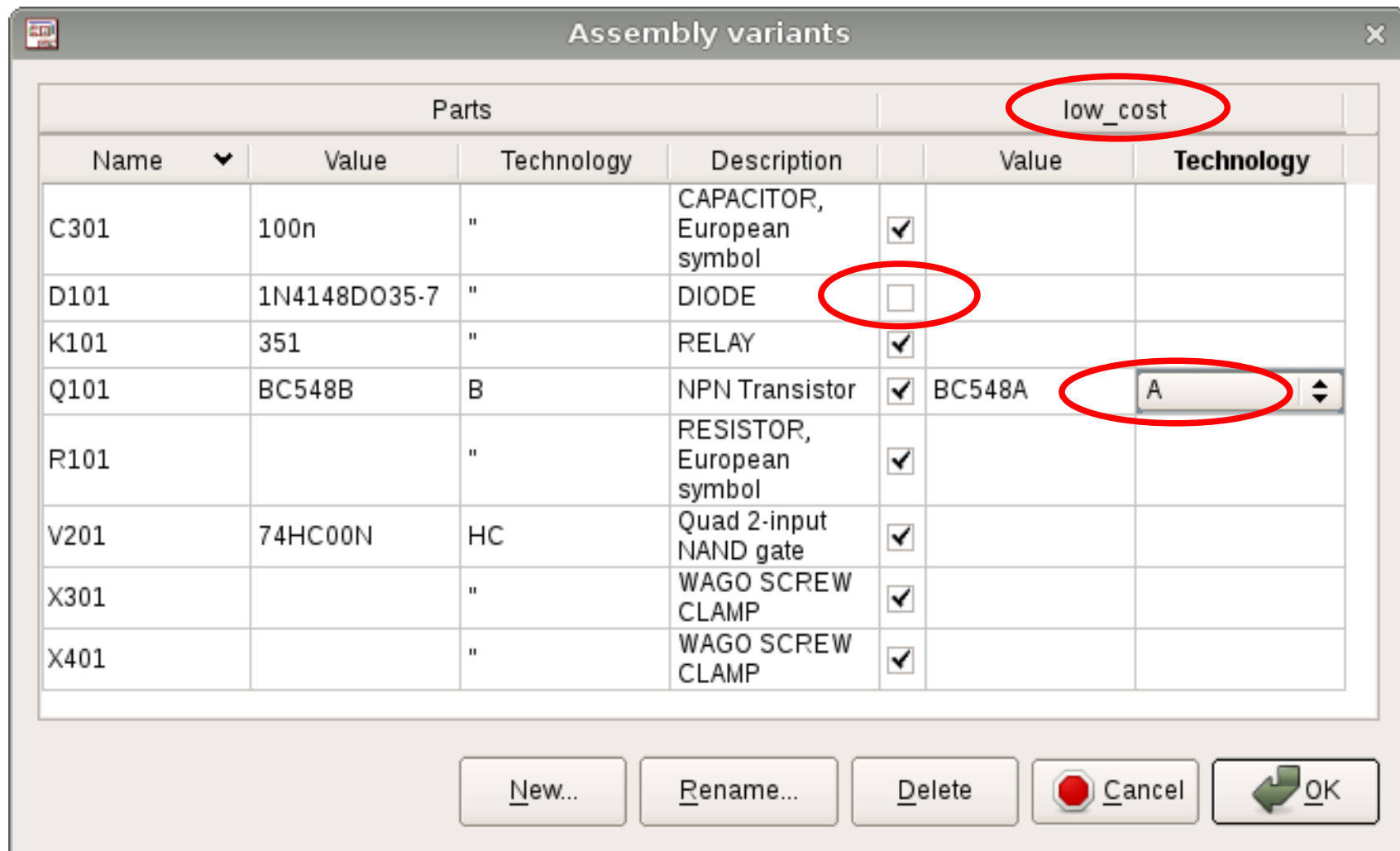


Bauteilnamen

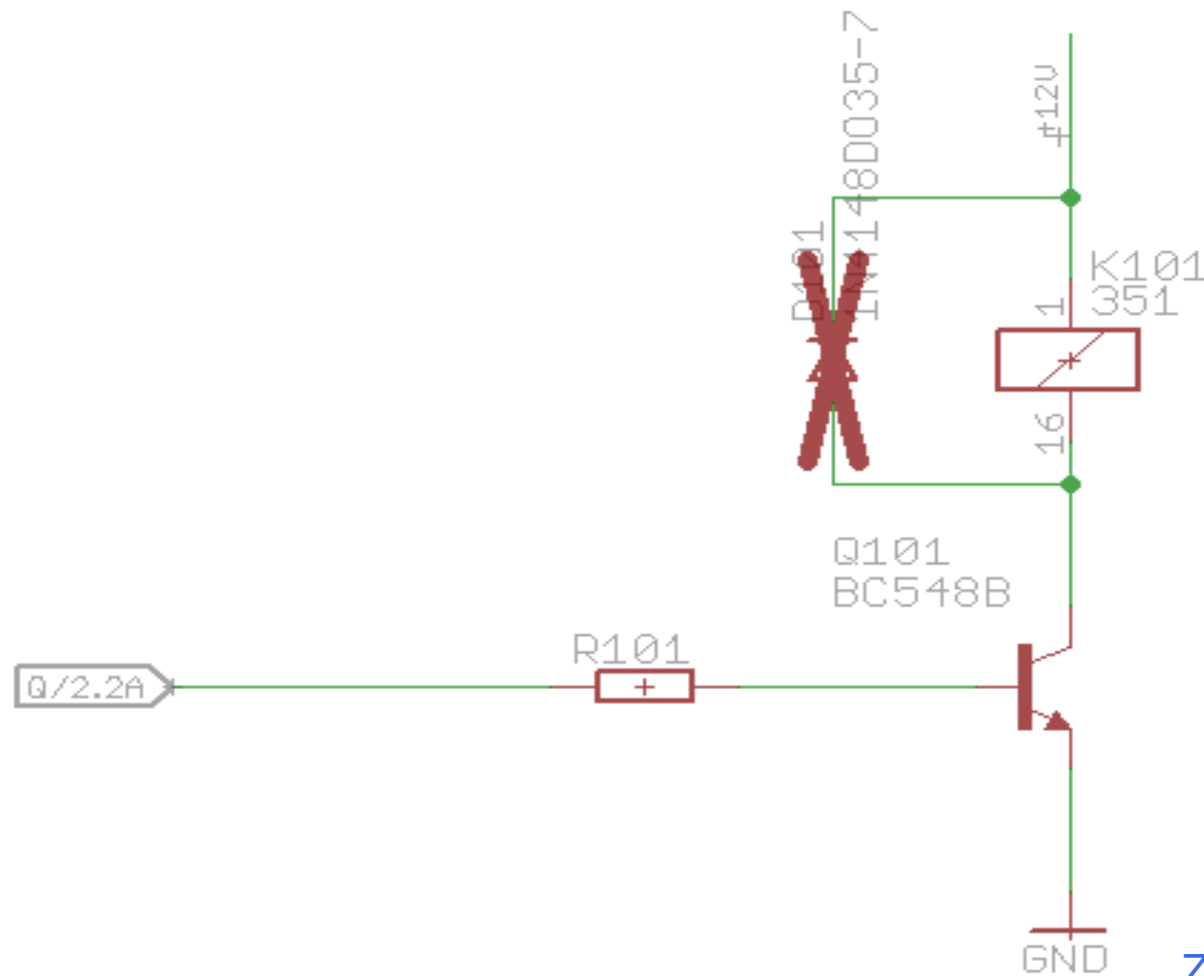
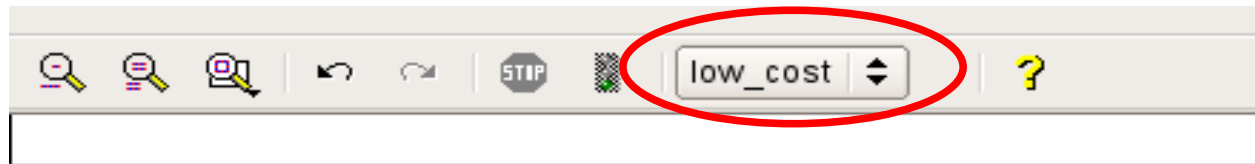


Bestückungsvarianten #1

Befehl VARIANT



Bestückungsvarianten #2



Zeichnungsnummer
beachten !

ERC

Befehle **ERC**, **ERROR**

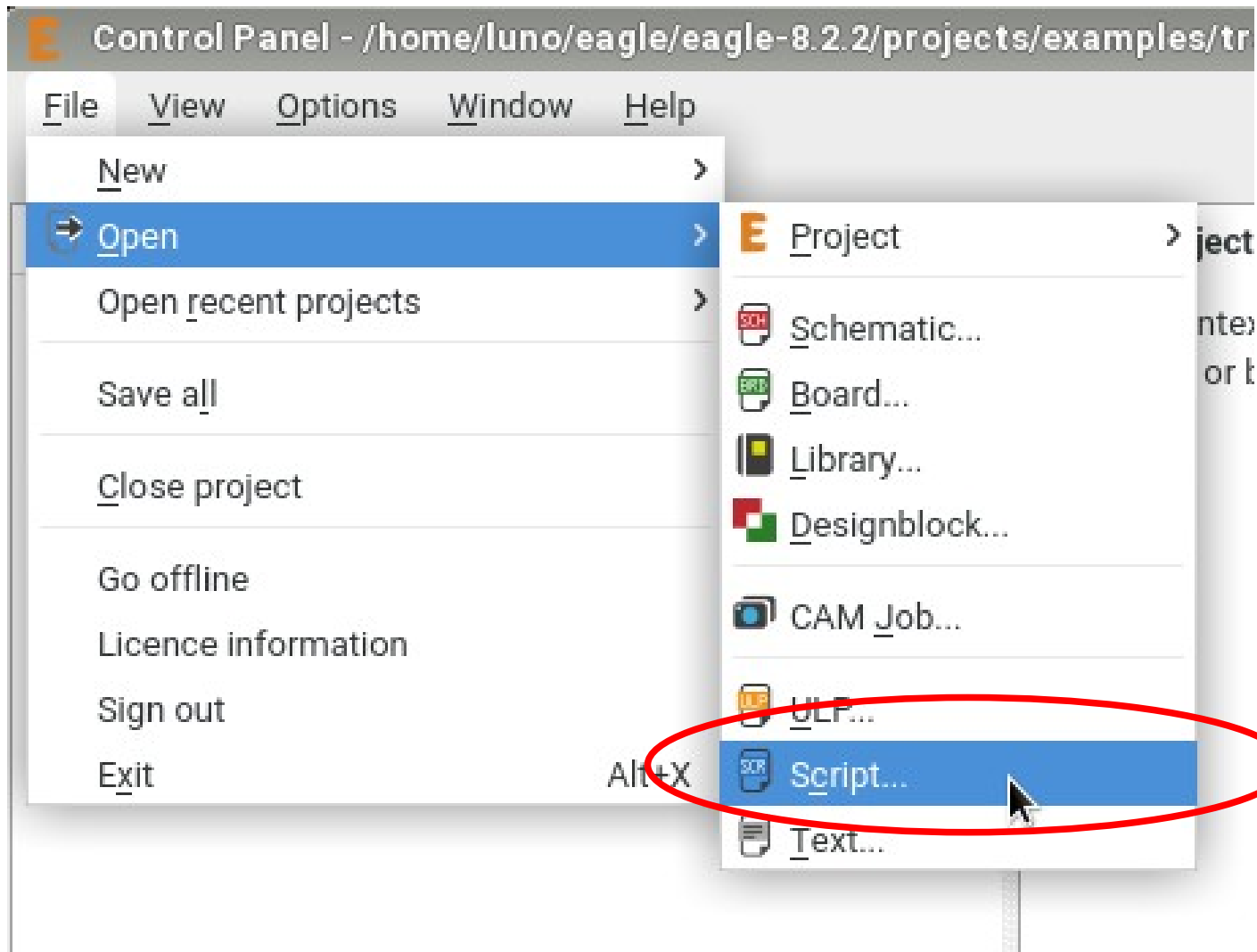
The screenshot shows the 'ERC Errors' dialog box. It has a title bar with 'SCH' on the left and window controls on the right. The main area contains a table with columns 'Type', 'Sheet', and 'Module'. The table is organized into sections: 'Consistency not checked (no board loaded)', 'Errors (6)', and 'Warnings (17)'. Each entry in the table is preceded by a warning icon (red triangle with exclamation mark for errors, yellow triangle for warnings). At the bottom, there are four buttons: 'Centered' (with a checkbox), 'Processed', 'Approve', and 'Clear all'.

Type	Sheet	Module
Consistency not checked (no board loaded)		
<input type="checkbox"/> Errors (6)		
No SUPPLY for implicit POWER pin V1/+UB +UB	1	
No SUPPLY for implicit POWER pin V1/-UB -UB	1	
Only INPUT pins on net CLK	1	
Only INPUT pins on net CLK#	1	
Unconnected INPUT pin V1/2 A	1	
Unconnected INPUT pin V1/2 B	1	
<input type="checkbox"/> Warnings (17)		
Only one pin on net !Q	1	
Only one pin on net CLK	1	
Only one pin on net CLK#	1	
Part C1 has no value	1	
Part C2 has no value	1	
Part C3 has no value	2	

Centered

Processed Approve Clear all

SKRIPTE #1



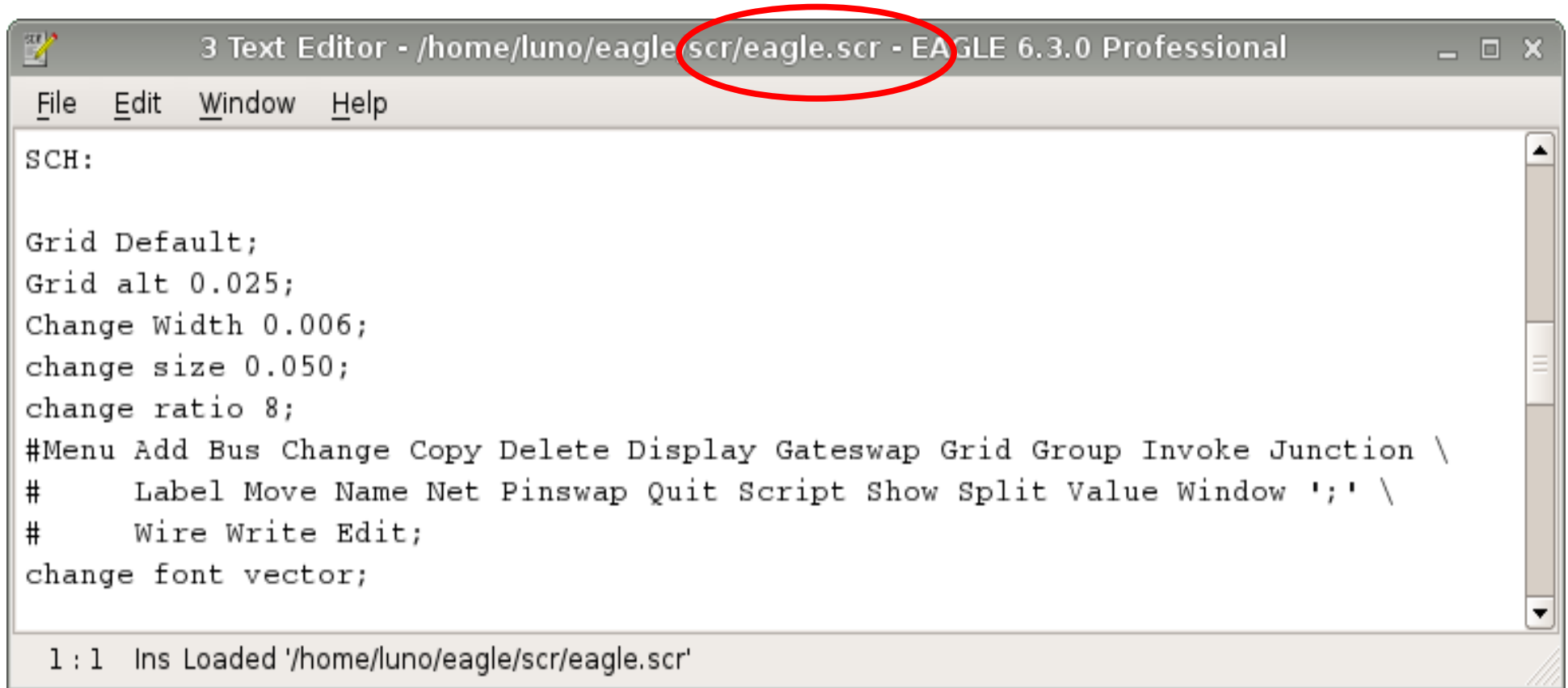
SKRIPTTE #2

The image shows a screenshot of the Eagle CAD software interface. The main window is titled "Control Panel - /home/luno/eagle/eagle-8". The "Options" menu is open, and the "Directories..." option is highlighted. A red arrow labeled "1." points to this menu item. The "Directories" dialog box is open, showing various configuration fields. The "Scripts" field contains the text "\$EAGLEDIR/scr|" and is circled in red. A second red arrow labeled "2." points to this field. The dialog box also shows fields for Documentation, Libraries, Design Blocks, Design Rules, User Language Programs, CAM Jobs, and Projects, each with a corresponding path starting with "\$EAGLEDIR/".

Category	Path
Documentation	\$EAGLEDIR/doc
Libraries	\$EAGLEDIR/lbr
Design Blocks	\$EAGLEDIR/dbl
Design Rules	\$EAGLEDIR/dru
User Language Programs	\$EAGLEDIR/ulp
Scripts	\$EAGLEDIR/scr
CAM Jobs	\$EAGLEDIR/cam
Projects	\$HOME/eagle:\$EAGLEDIR/projects/examples

1. 2.

SKRIPTE #3



```
3 Text Editor - /home/luno/eagle/src/eagle.scr - EAGLE 6.3.0 Professional
File Edit Window Help
SCH:

Grid Default;
Grid alt 0.025;
Change Width 0.006;
change size 0.050;
change ratio 8;
#Menu Add Bus Change Copy Delete Display Gateswap Grid Group Invoke Junction \
#   Label Move Name Net Pinswap Quit Script Show Split Value Window ';' \
#   Wire Write Edit;
change font vector;

1:1 Ins Loaded '/home/luno/eagle/src/eagle.scr'
```

Ausführung automatisch bei EAGLE Start !

https://github.com/Blunk-electronic/lbr_eagle/blob/master/src/eagle.scr

SKRIPTE #4

Mehr zu EAGLE-Skripten hier :

Scripting Tutorial

http://www.blunk-electronic.de/pdf/Scripting_de.pdf

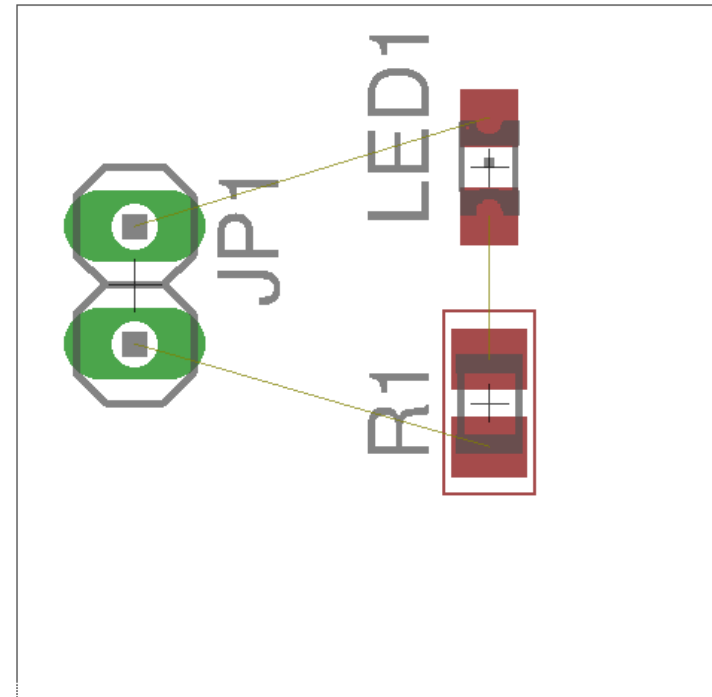
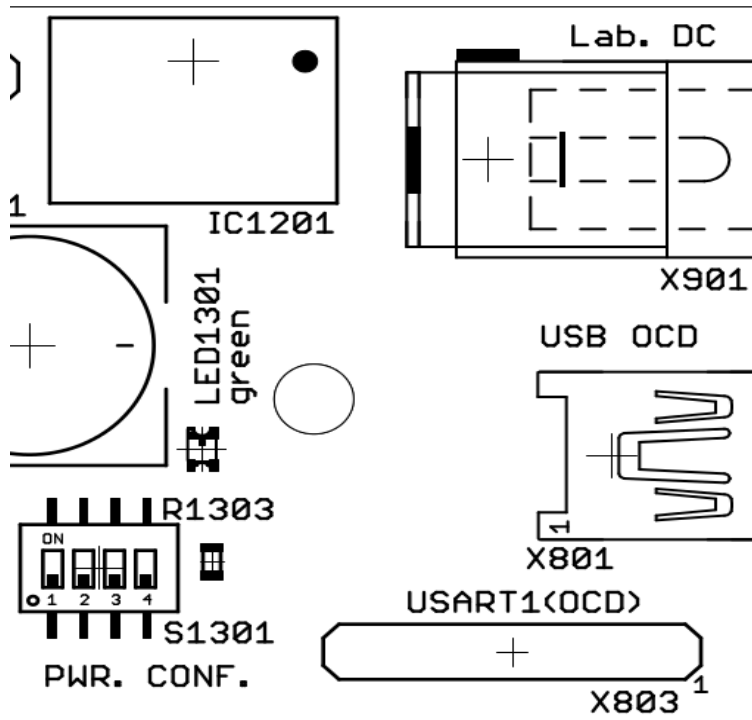
Leiterplatte #1



Thanks to: Key Design Electronics Ltd. <http://www.kdel.co.uk/>
26 Lancaster Way, Scalby, Scarborough, YO13 0QH, England
+44 (0) 1723 341809

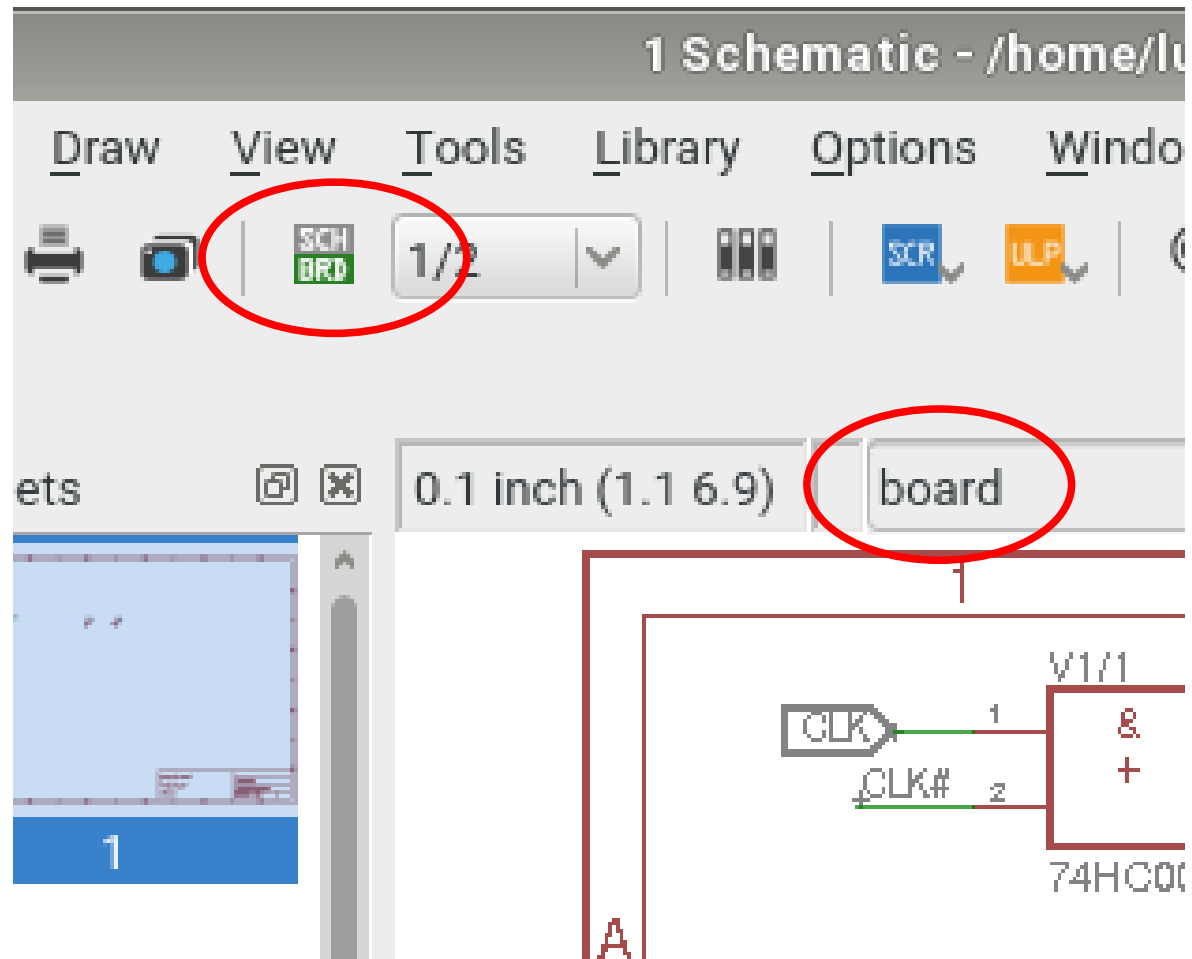
Leiterplatte #2

Synonyme: Baugruppe, PCBA (Printed Circuit Board Assembled)



Board erzeugen

Befehl
Board

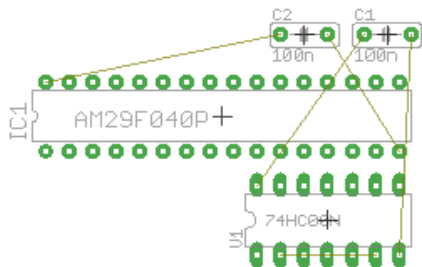


Konturen

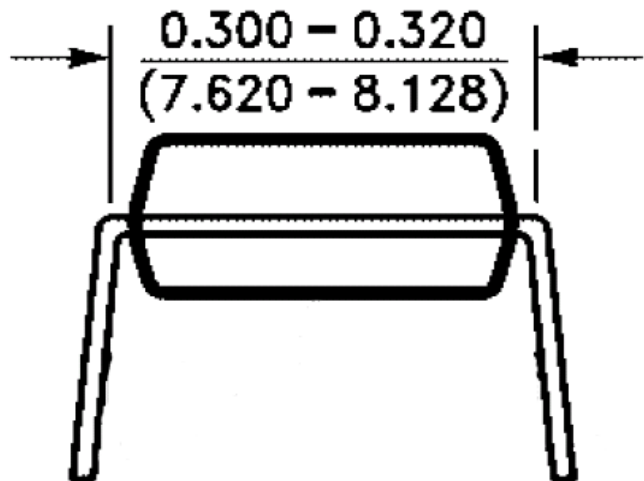
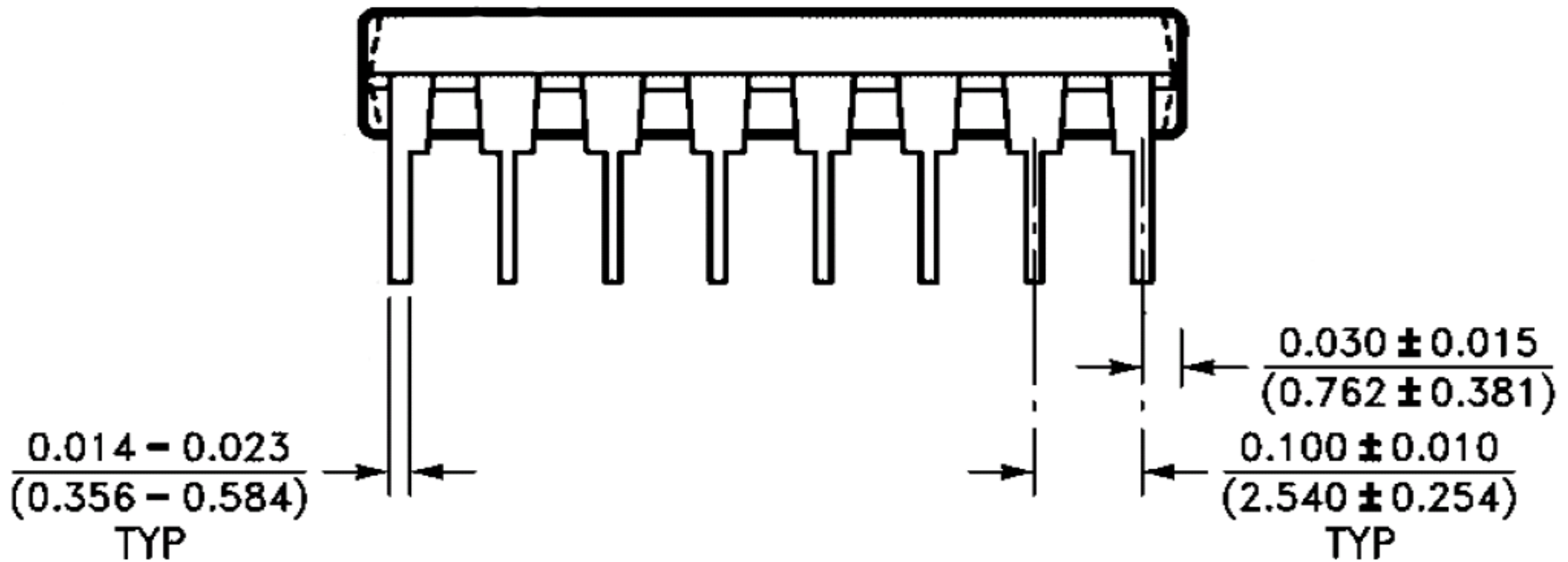
Befehle **MOVE**, **WIRE**, **SPLIT**, **DELETE**, **CIR**, **ARC**

\$ / €

Grid metrisch / inch ?



Metrisch & Zoll

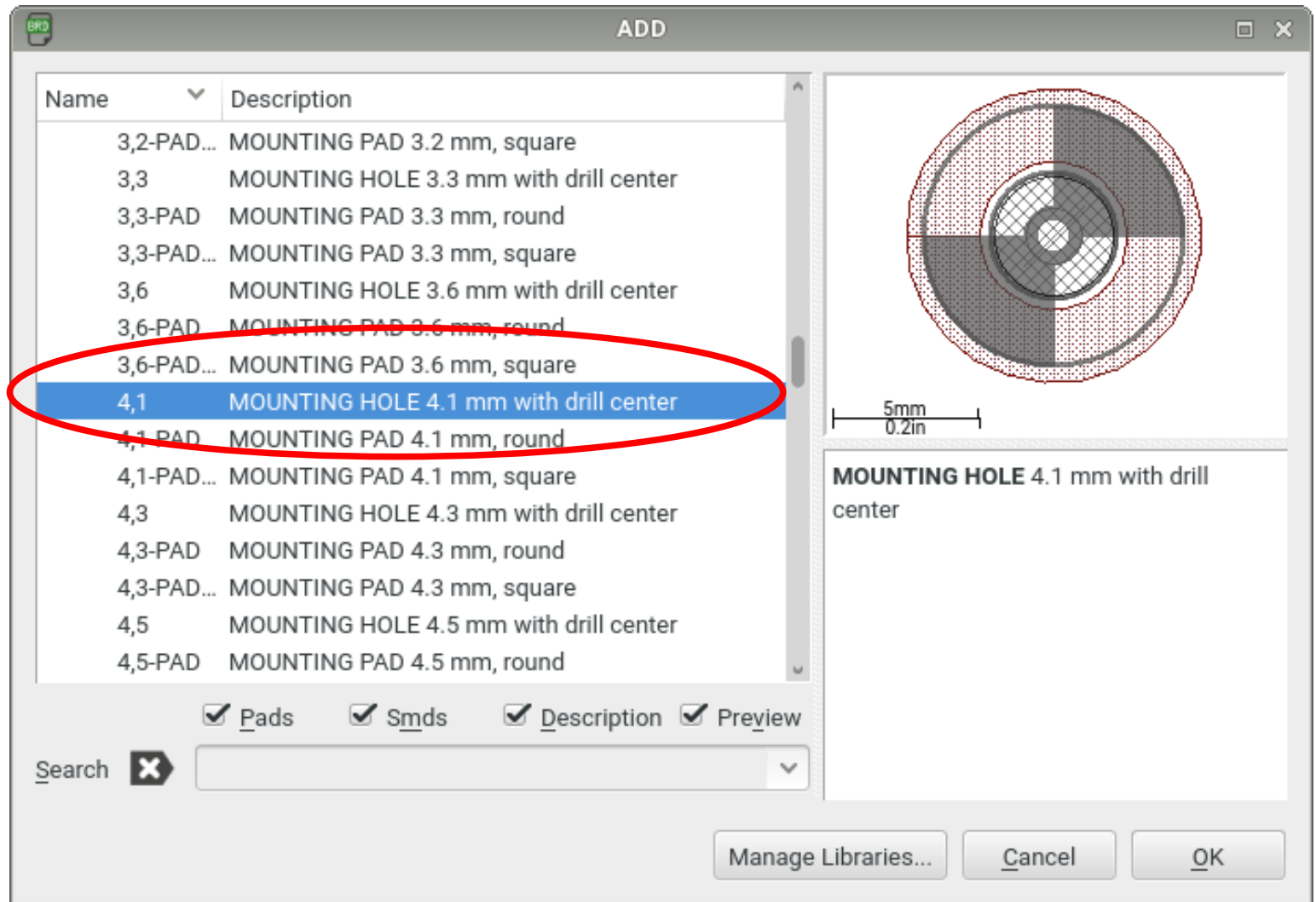


$$\frac{0.1 \text{ inch}}{2.54 \text{ mm}} = \frac{x \text{ inch gesucht}}{y \text{ mm gegeben}}$$

Bohrungen #1

Befehle

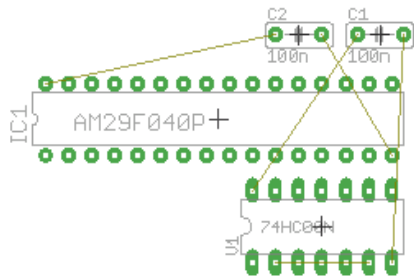
**ADD,
DELETE,
MOVE**



Bohrungen #2

Befehle

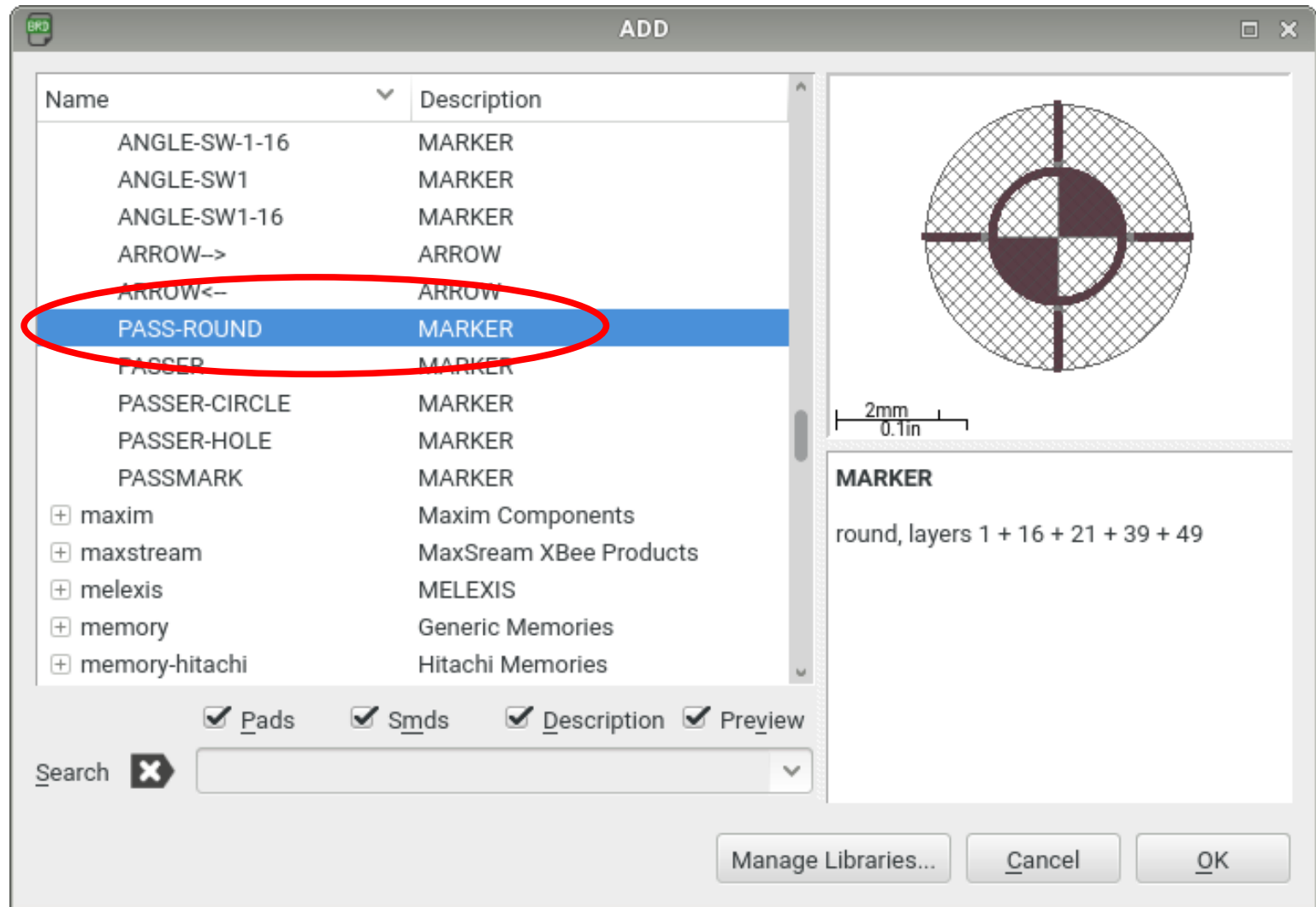
**COPY,
DELETE,
MOVE,
LOCK**



Grid
metrisch / inch ?

Passmarken / Fiducials #1

Befehl ADD

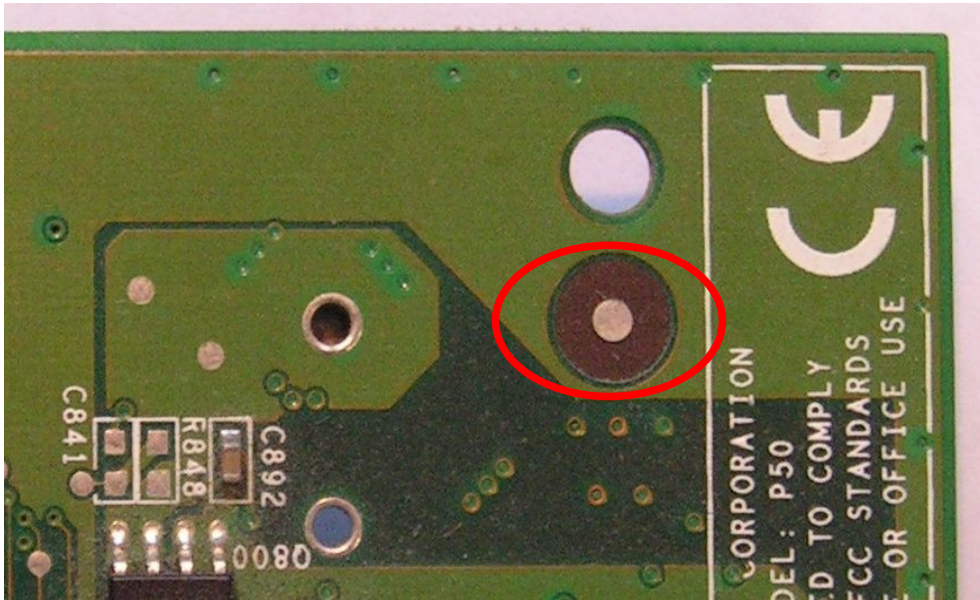


Passmarken / Fiducials #2

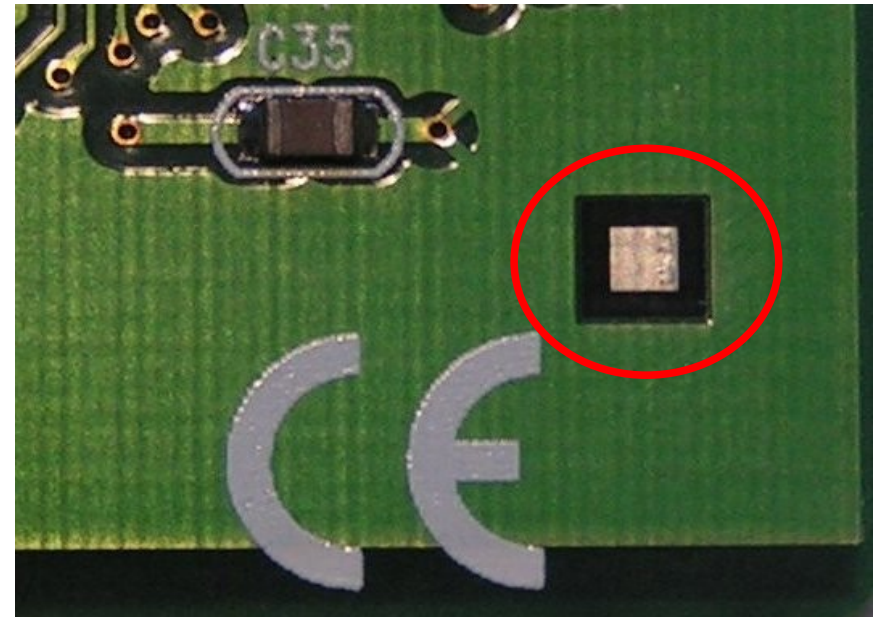
Befehle MOVE, DELETE, COPY, LOCK



Passmarken / Fiducials #3



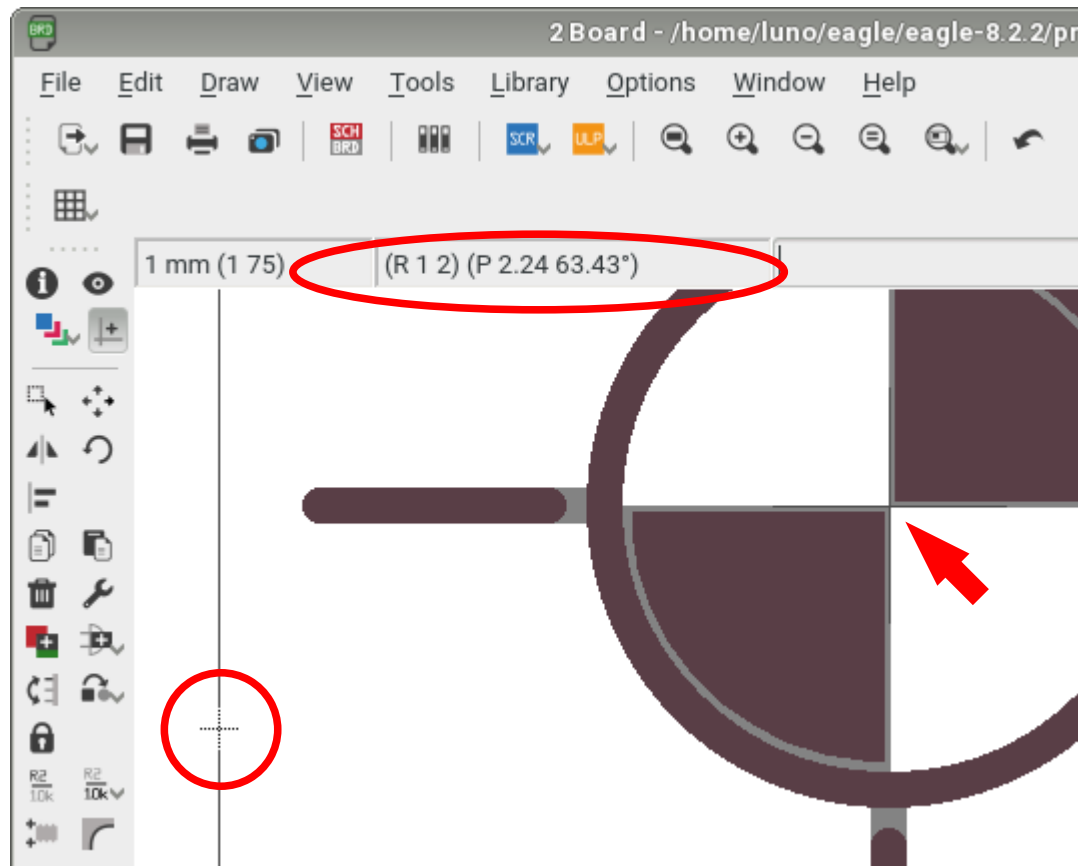
PCB- Bestücker
kontaktieren !



Koordinaten müssen in
Pick&Place Liste stehen !

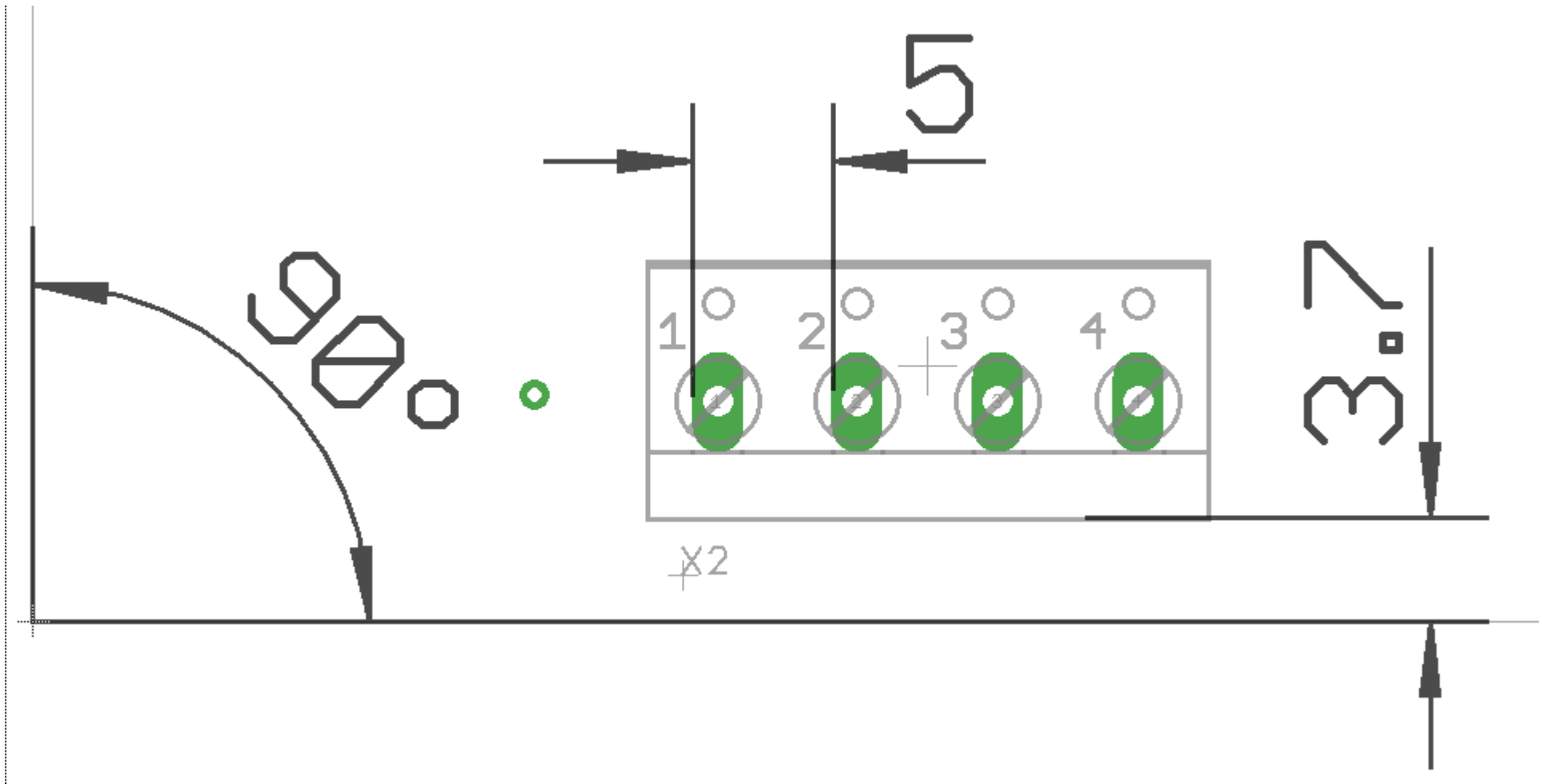
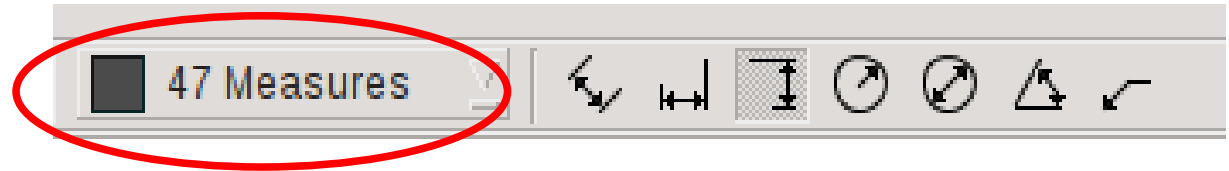
Abstandsmessungen #1

Befehle **MARK, MARK;**



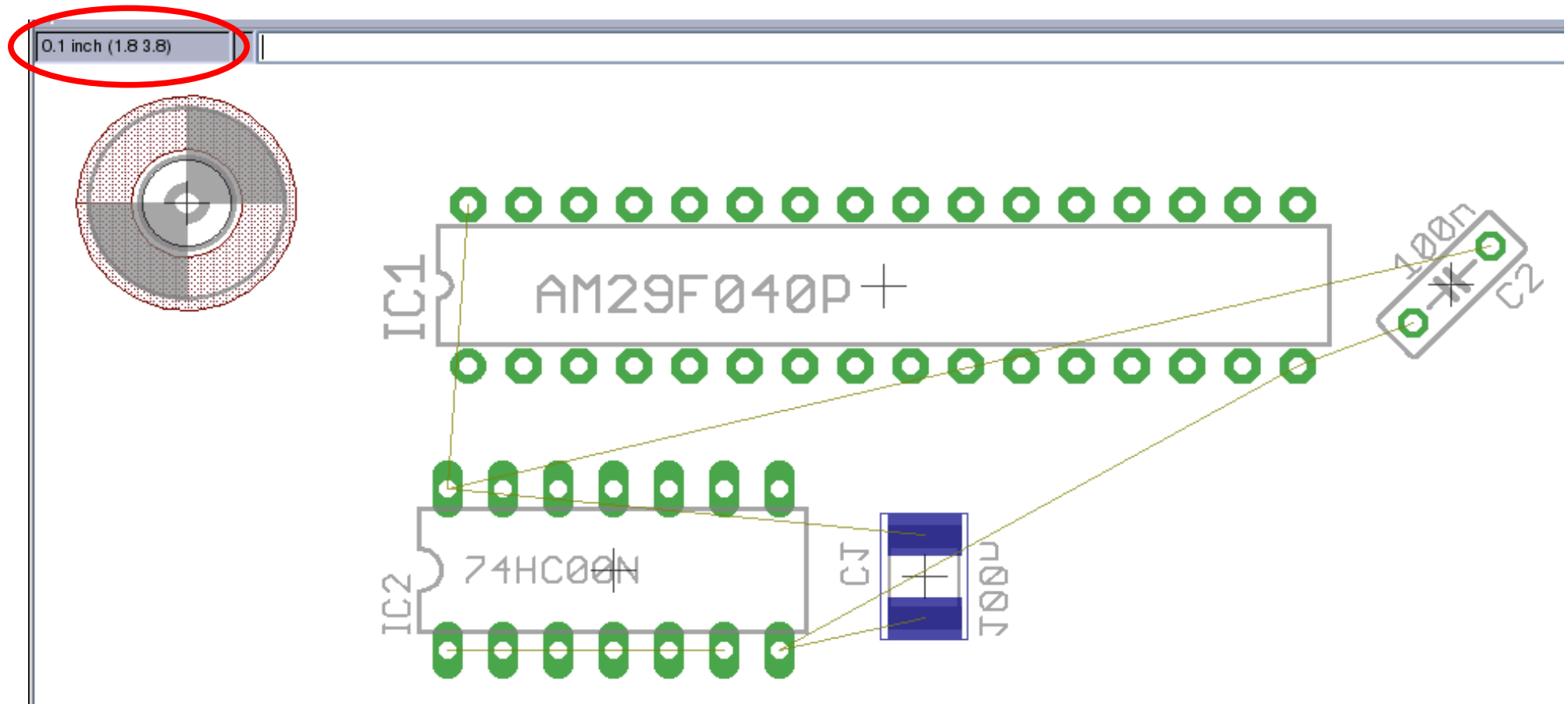
Abstandsmessungen #2

Befehl DIM

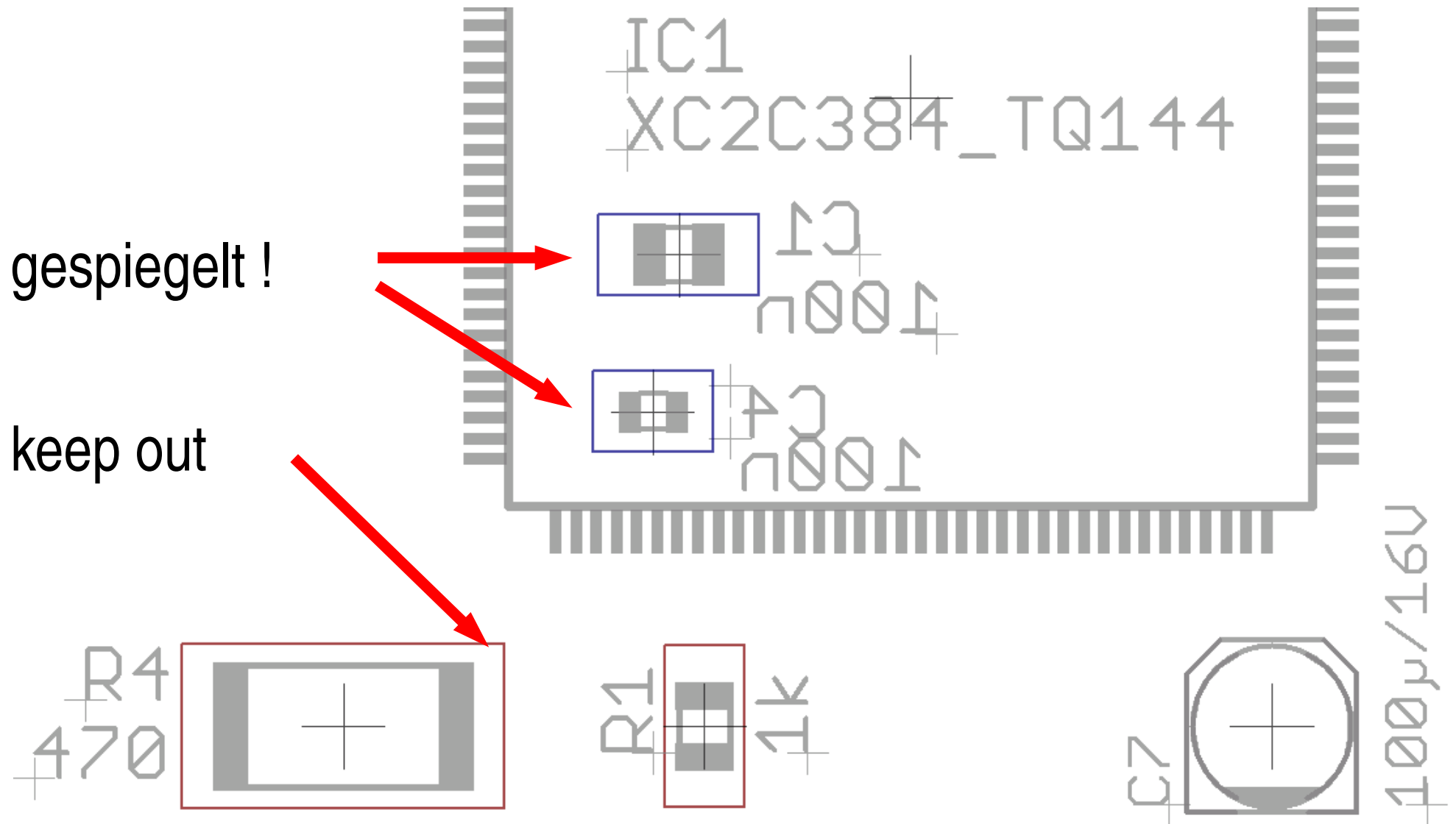


Bauteile platzieren #1

Befehle **LOCK**, **MOVE R77**, **GROUP**, **CHANGE**,
ROTATE R-45, **MIRROR**, **RATSNET**

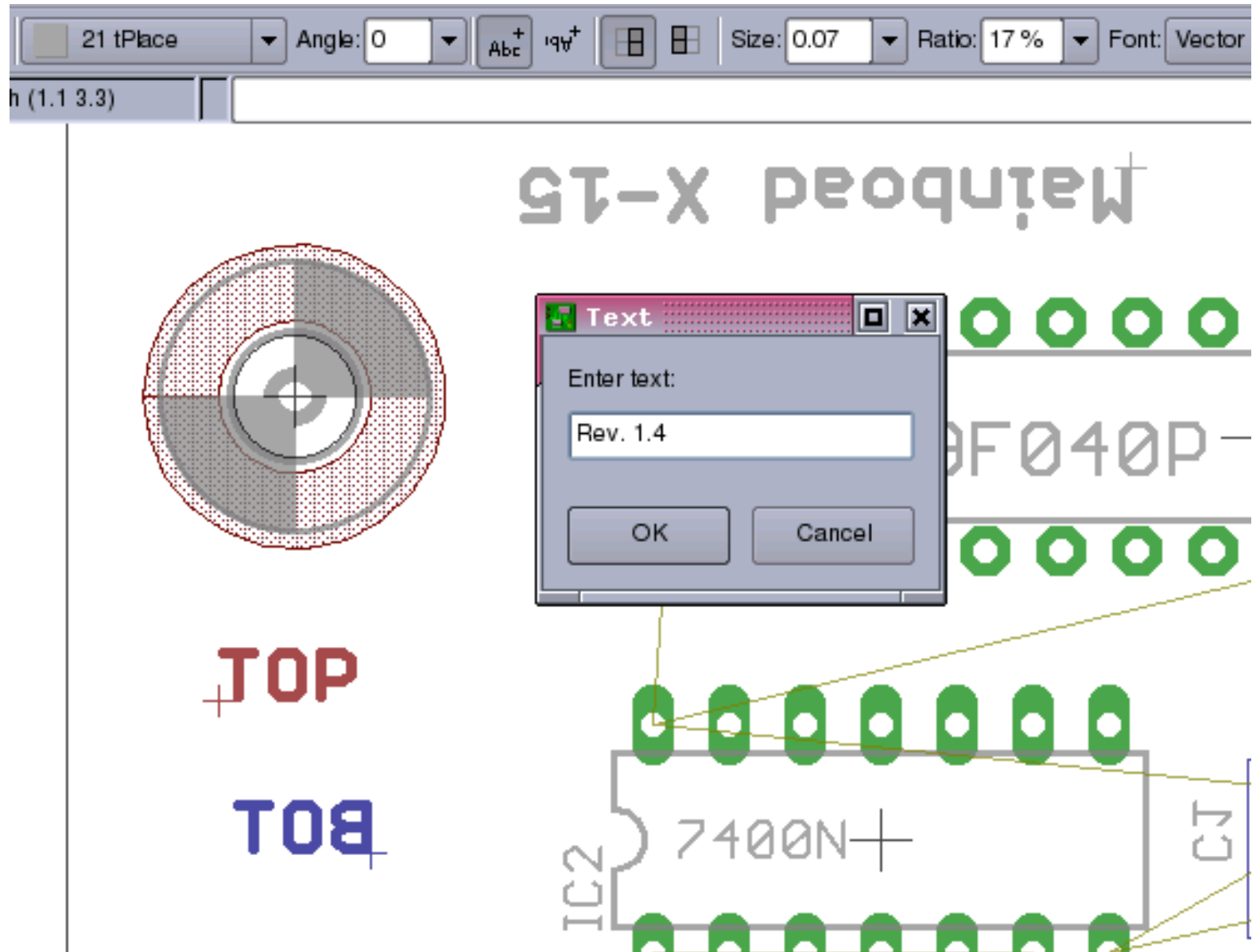


Bauteile platzieren #2

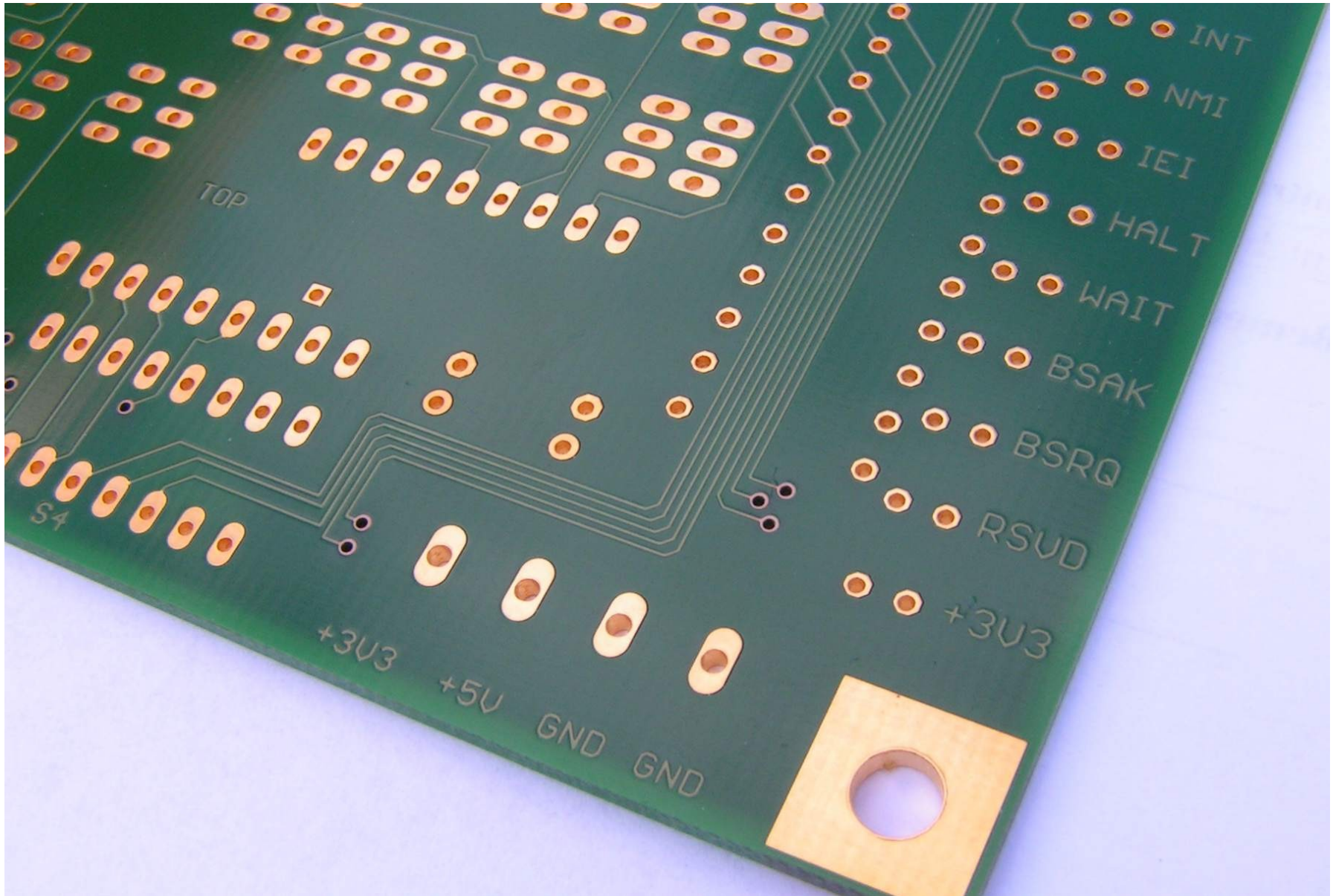


Texte #1

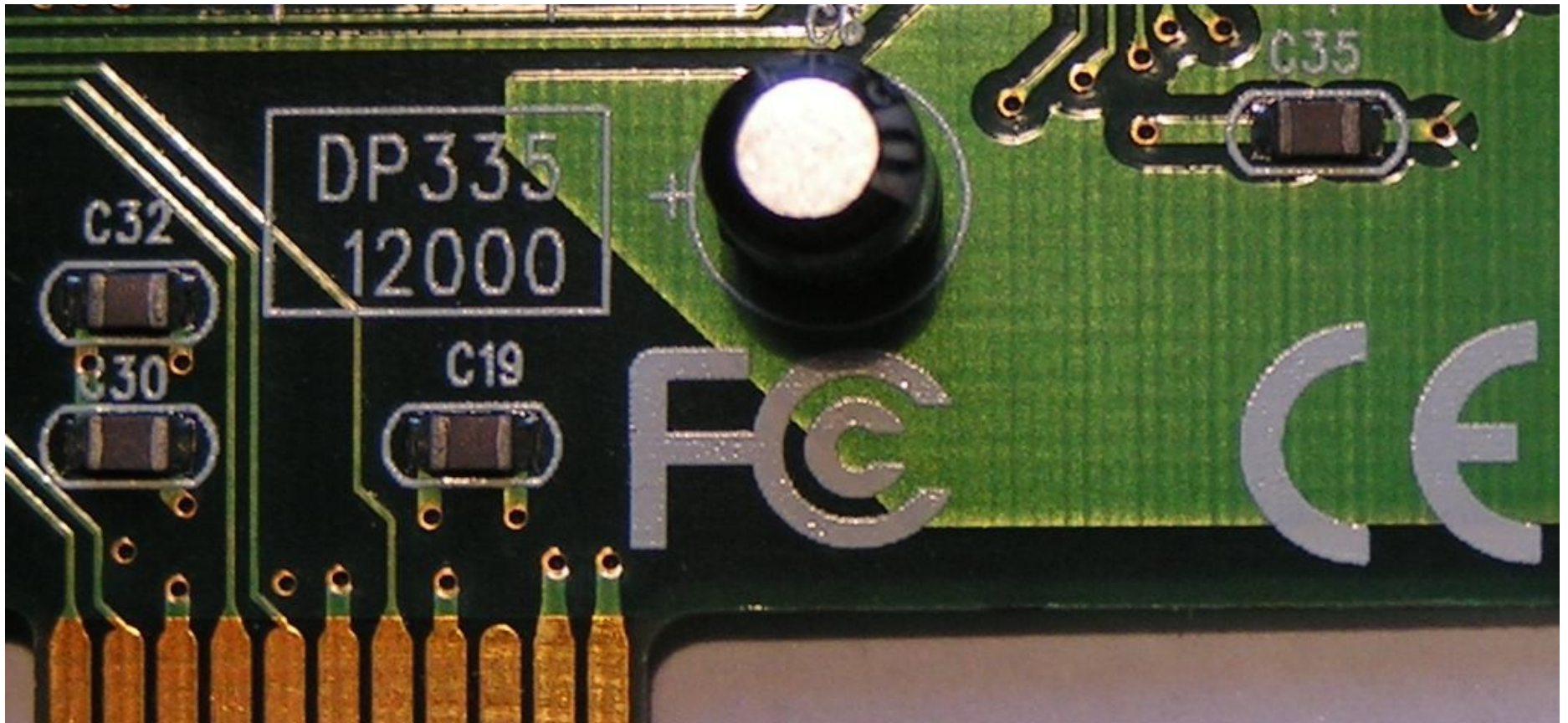
- Befehle
TEXT,
CHANGE
- TEXT
 - SIZE
 - RATIO
 - LAYER



Texte #2



Texte #3



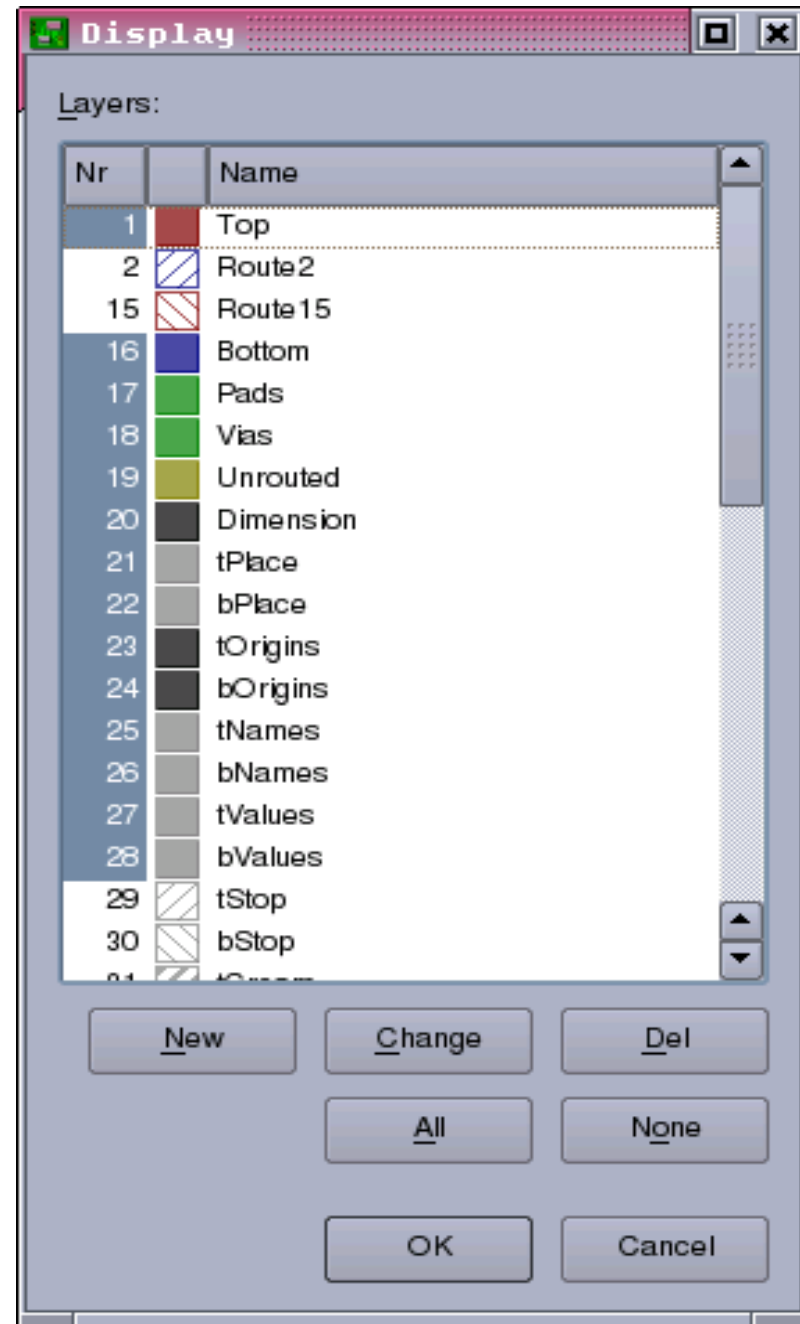
Board Layer

Befehle

DISPLAY,

LAYER

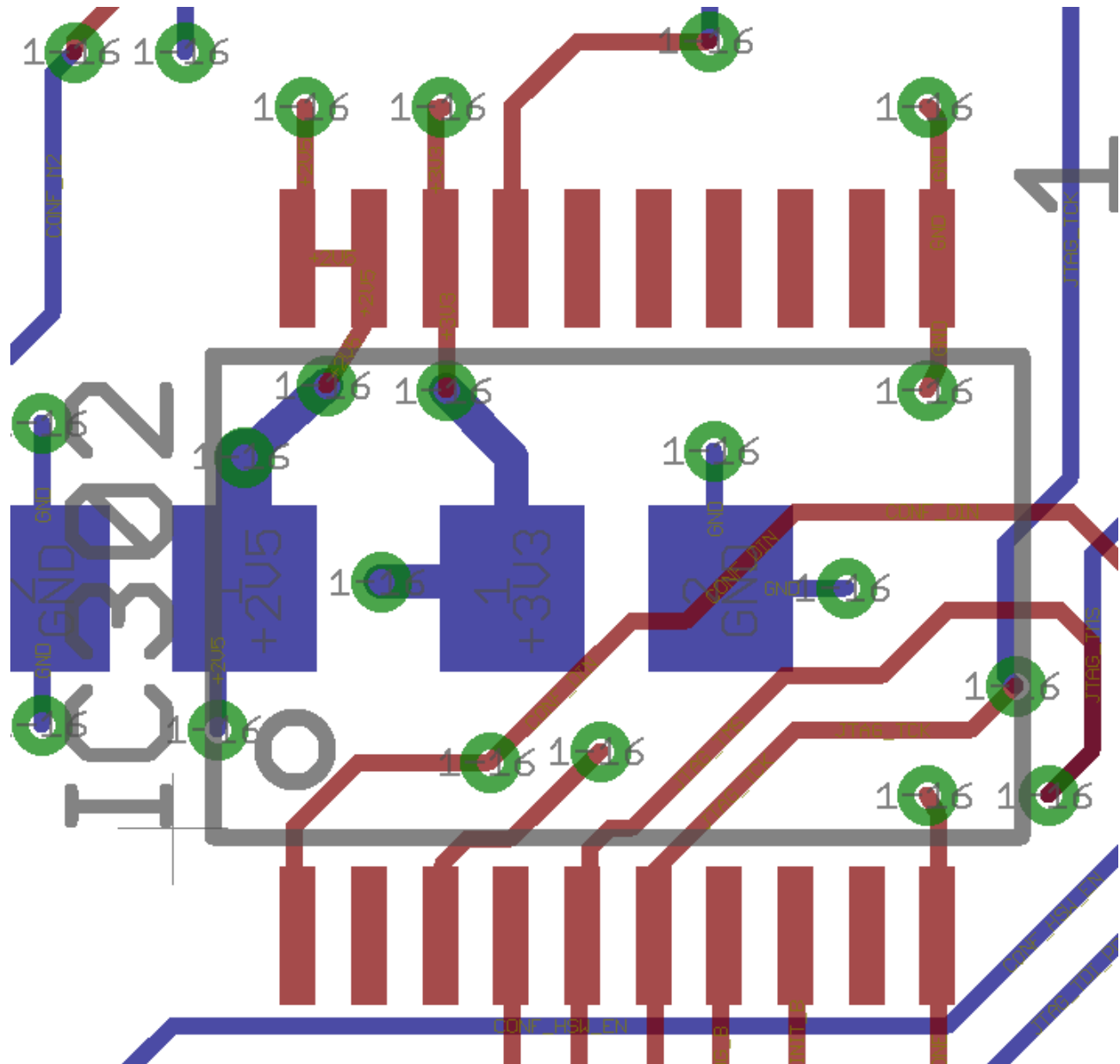
CHANGE LAYER



Routen #1

Befehle

**ROUTE,
WIRE,
SPLIT,
RIPUP,
RATSNET,
MOVE
VIA,
CHANGE**

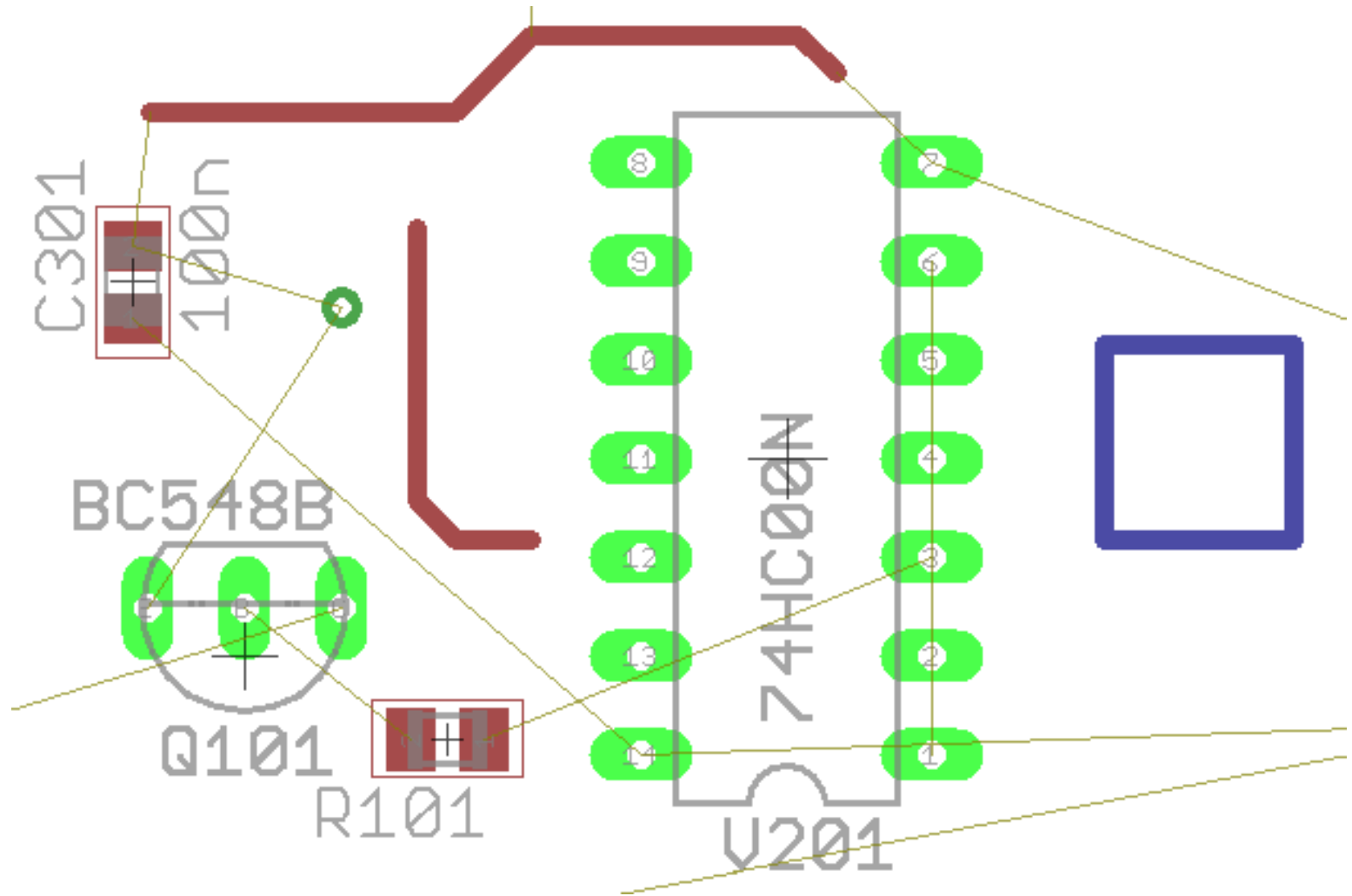


Router #2

Befehle

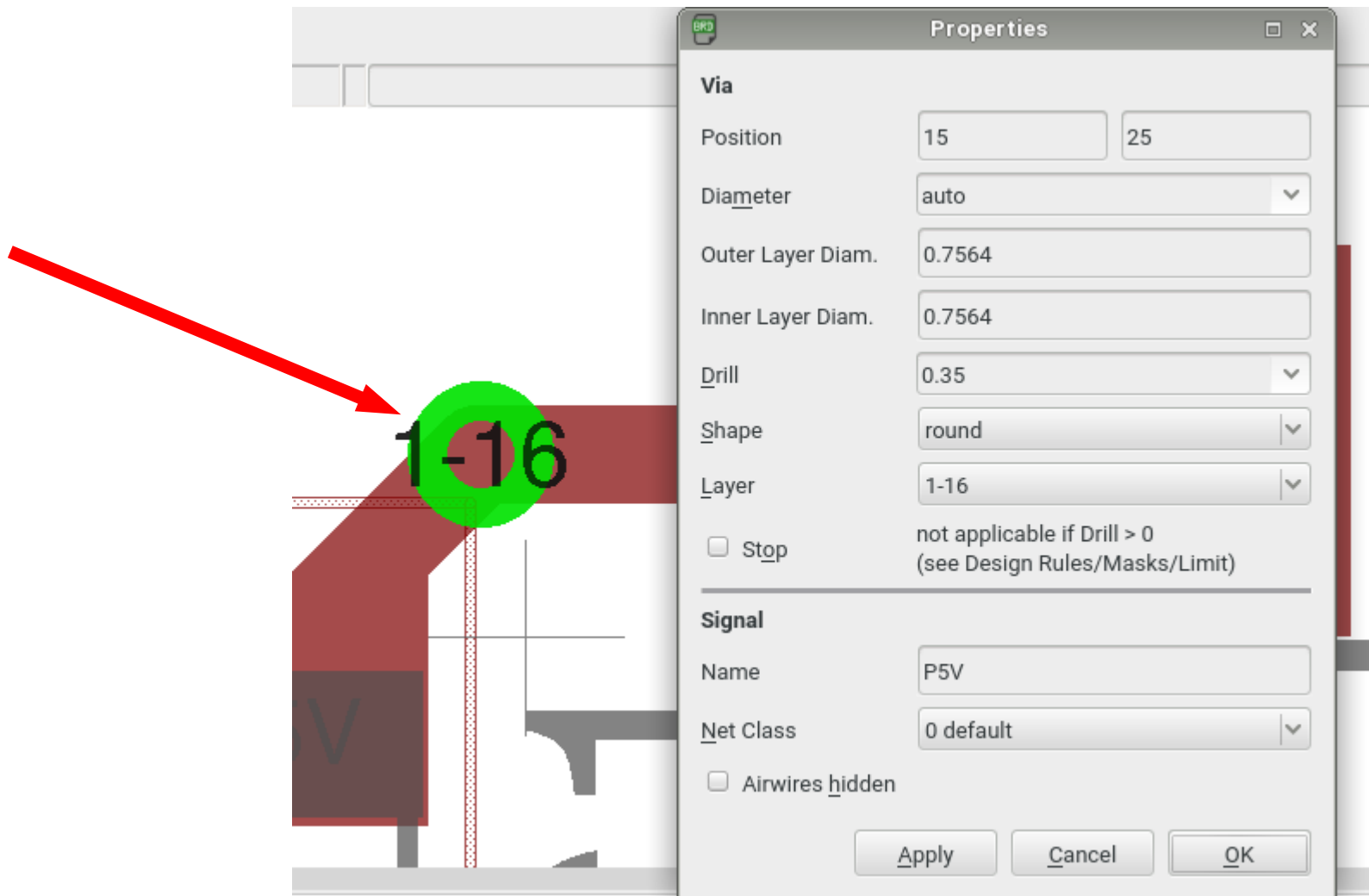
WIRE,
VIA
NAME,
RATSNET,

...

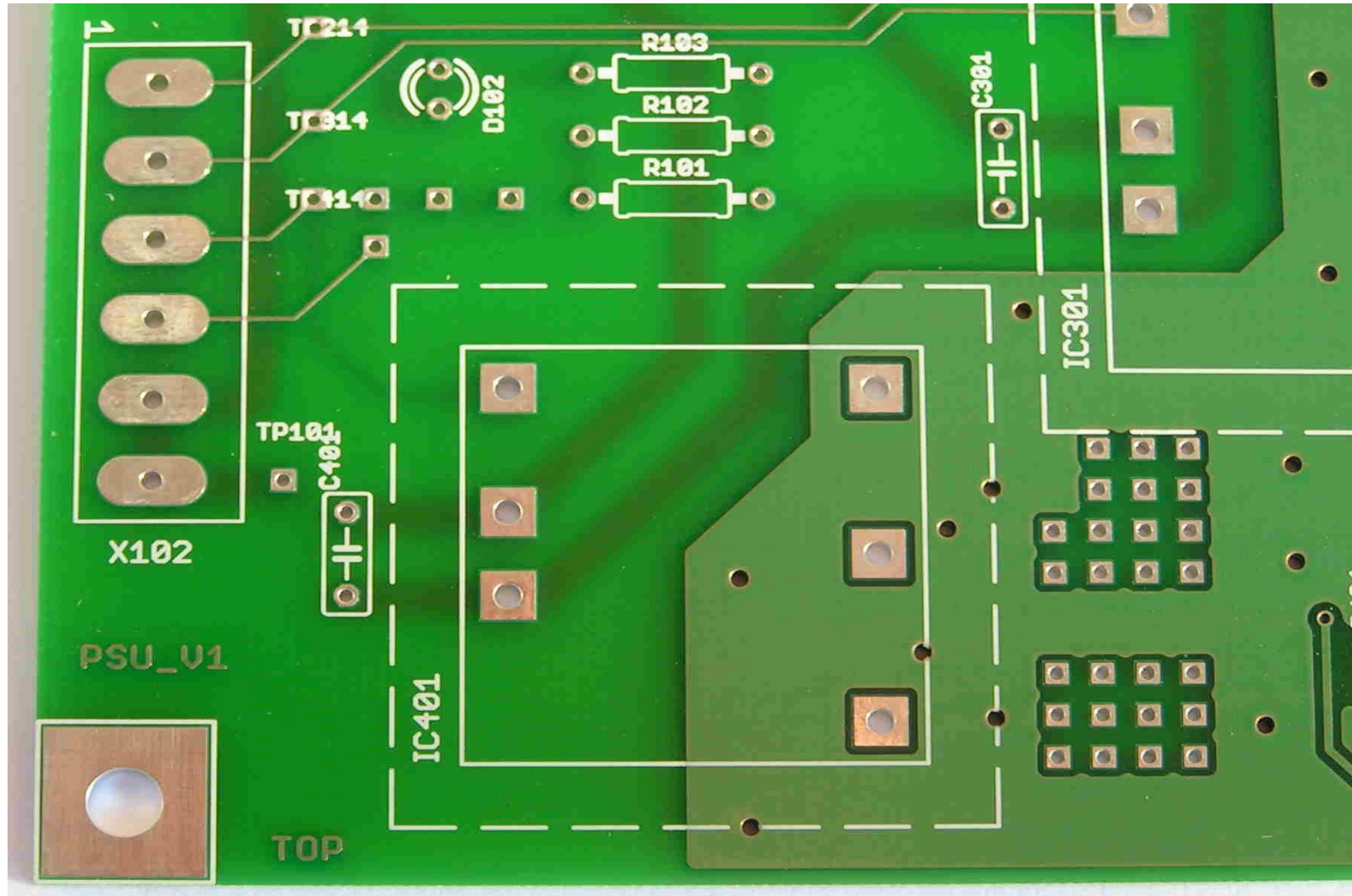


Via Eigenschaften

Befehle **INFO**, **CHANGE SHAPE / DIA / DRILL**

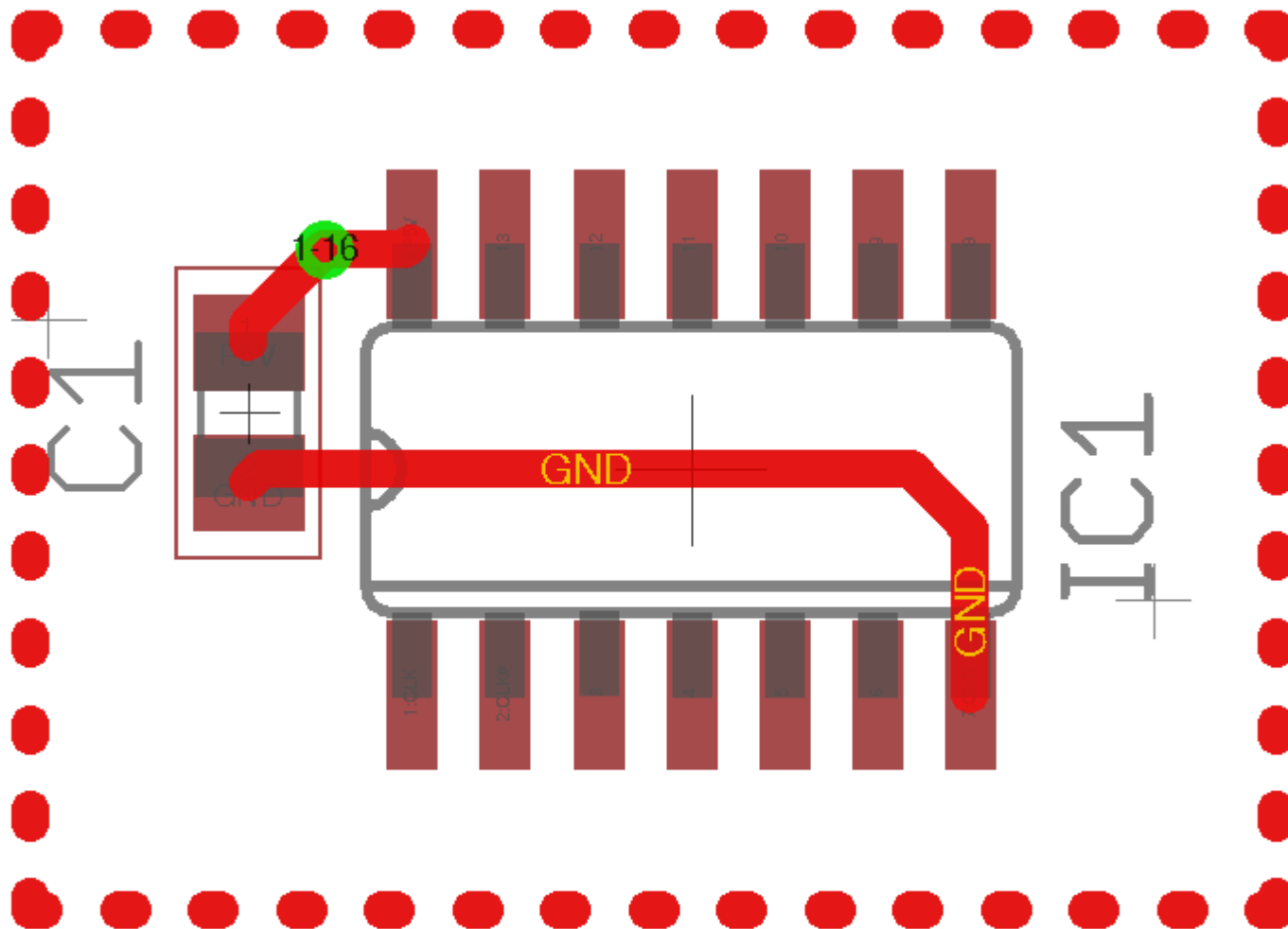


Polygone #1



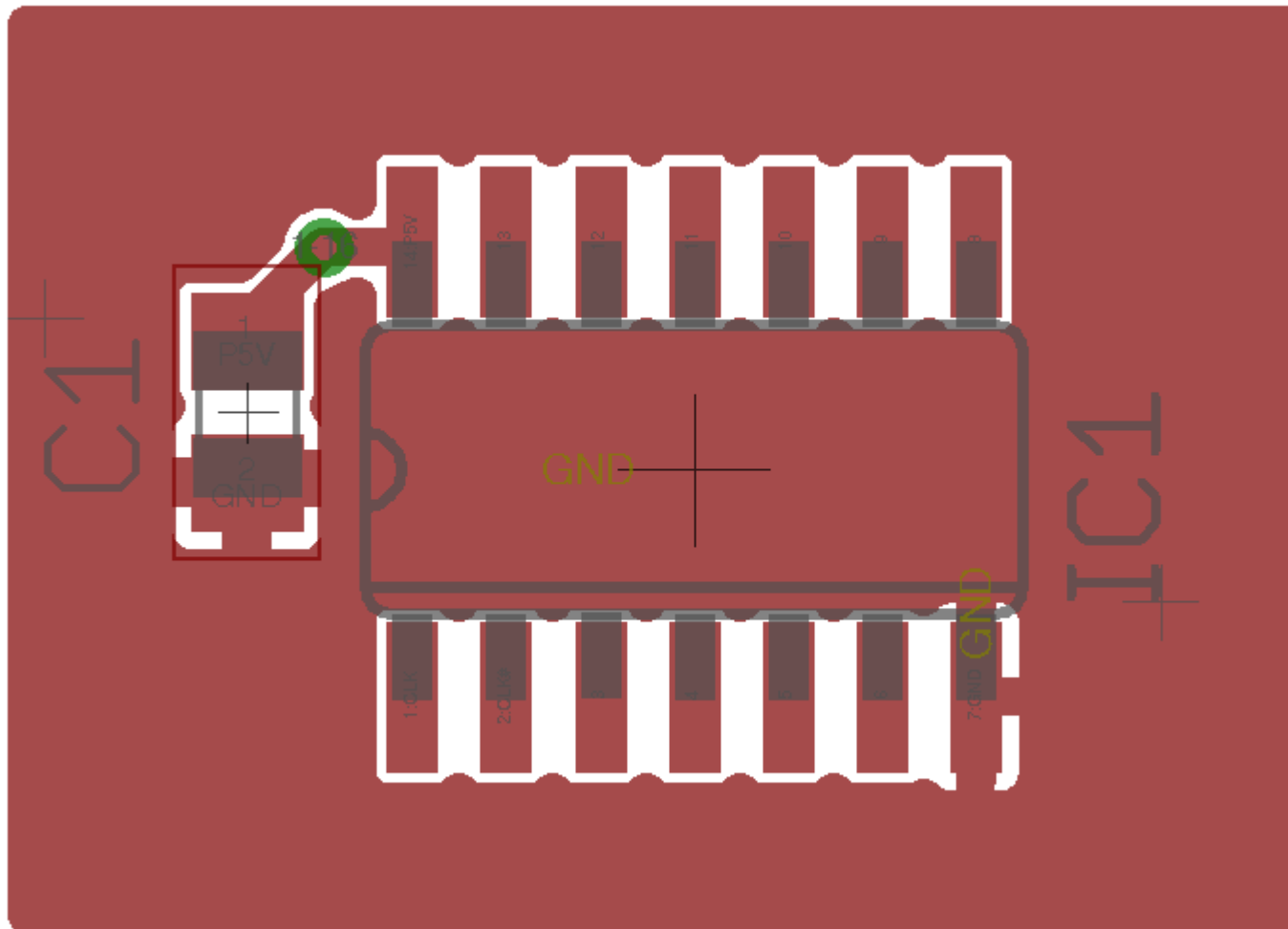
Polygone #2

Befehl **POLY, RATSNEST**



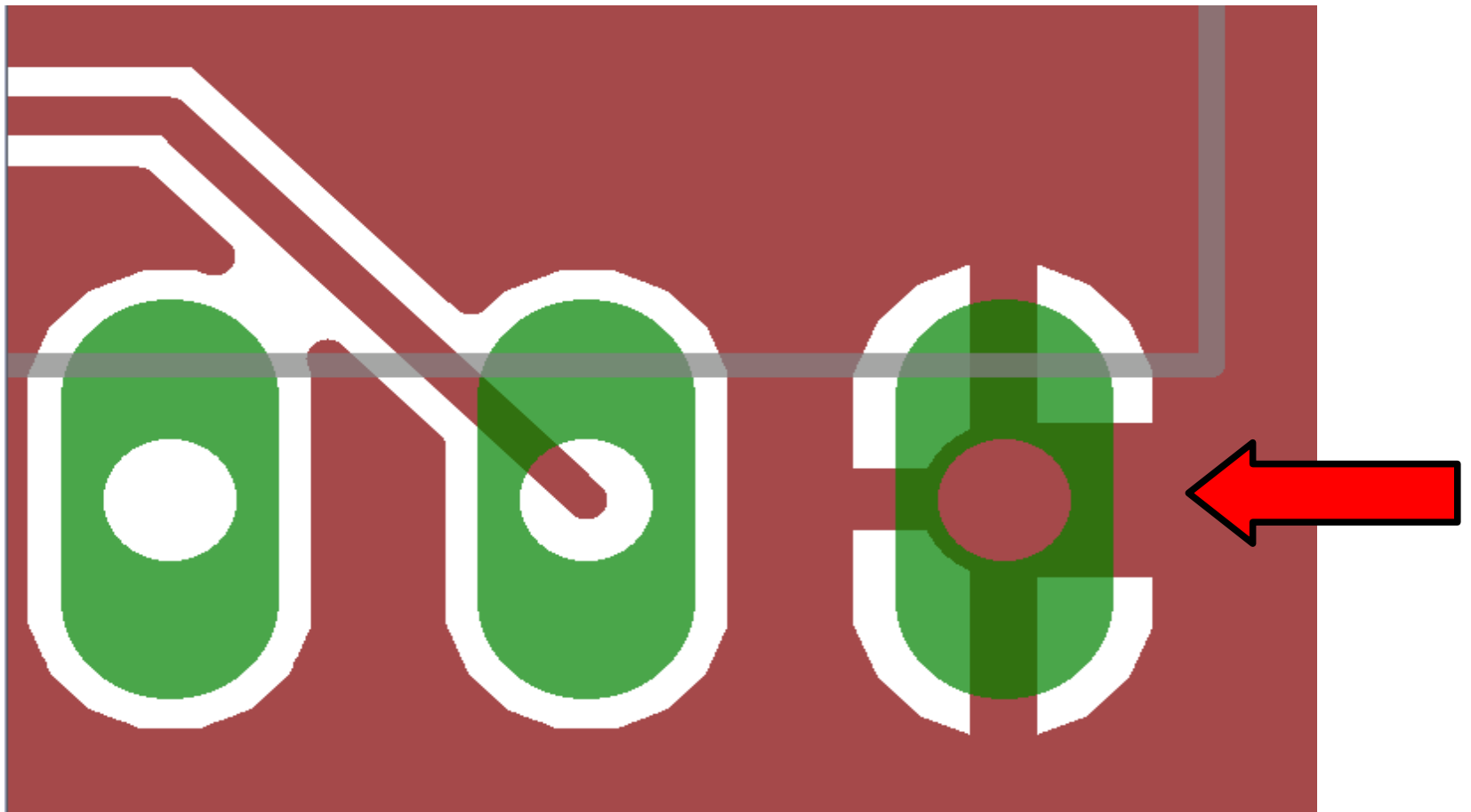
Polygone #3

Befehl **RATSNET, NAME, RIP @ yxz;**



Polygone #4

Befehl **CHANGE ISO / THERMAL / ORPHAN /
POUR / WIDTH, RIP @ xyz**



Autorouter #1

**Ein Autorouter bedarf Vorbereitungen und Grenzen für
brauchbare Ergebnisse !**

route alle Netze:

AUTO (nicht sinnvoll)

route alles außer:

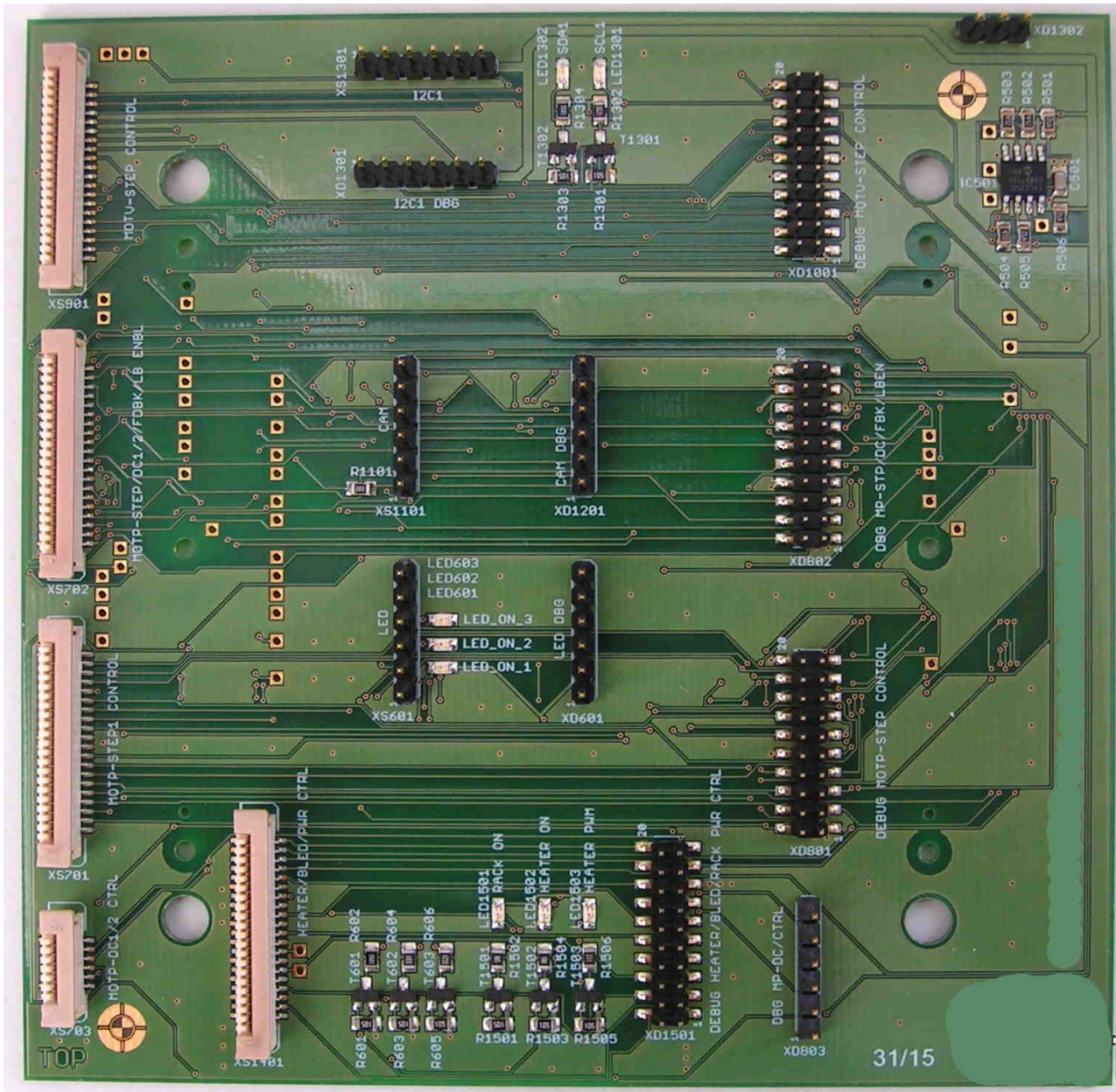
AUTO ! MASTER_CLOCK

route nur:

AUTO GPIO_*

Verwende Sperrgebiete
und Sperflächen !

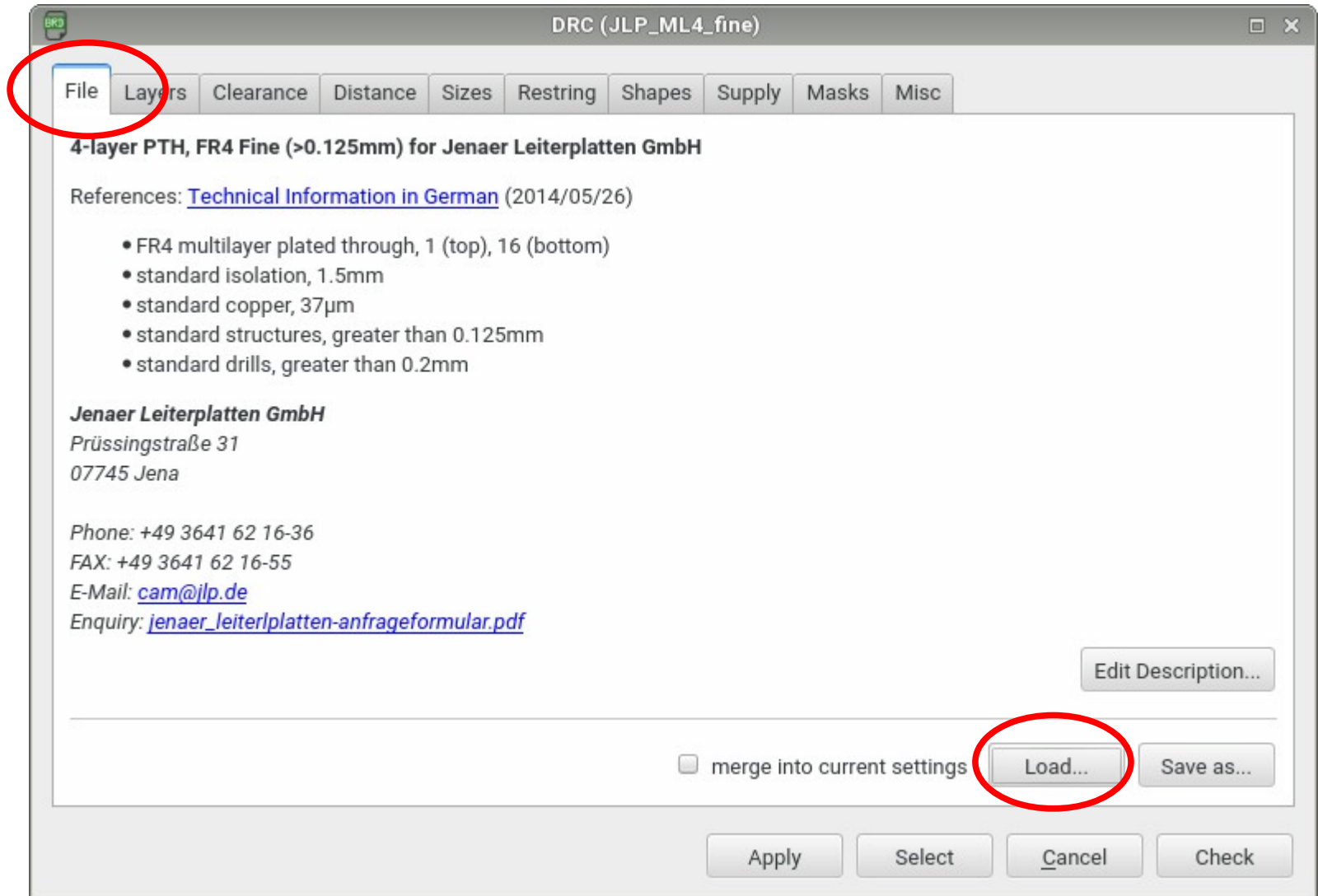
Autorouter #2



Nicht schön, aber schnell !

DRC #1

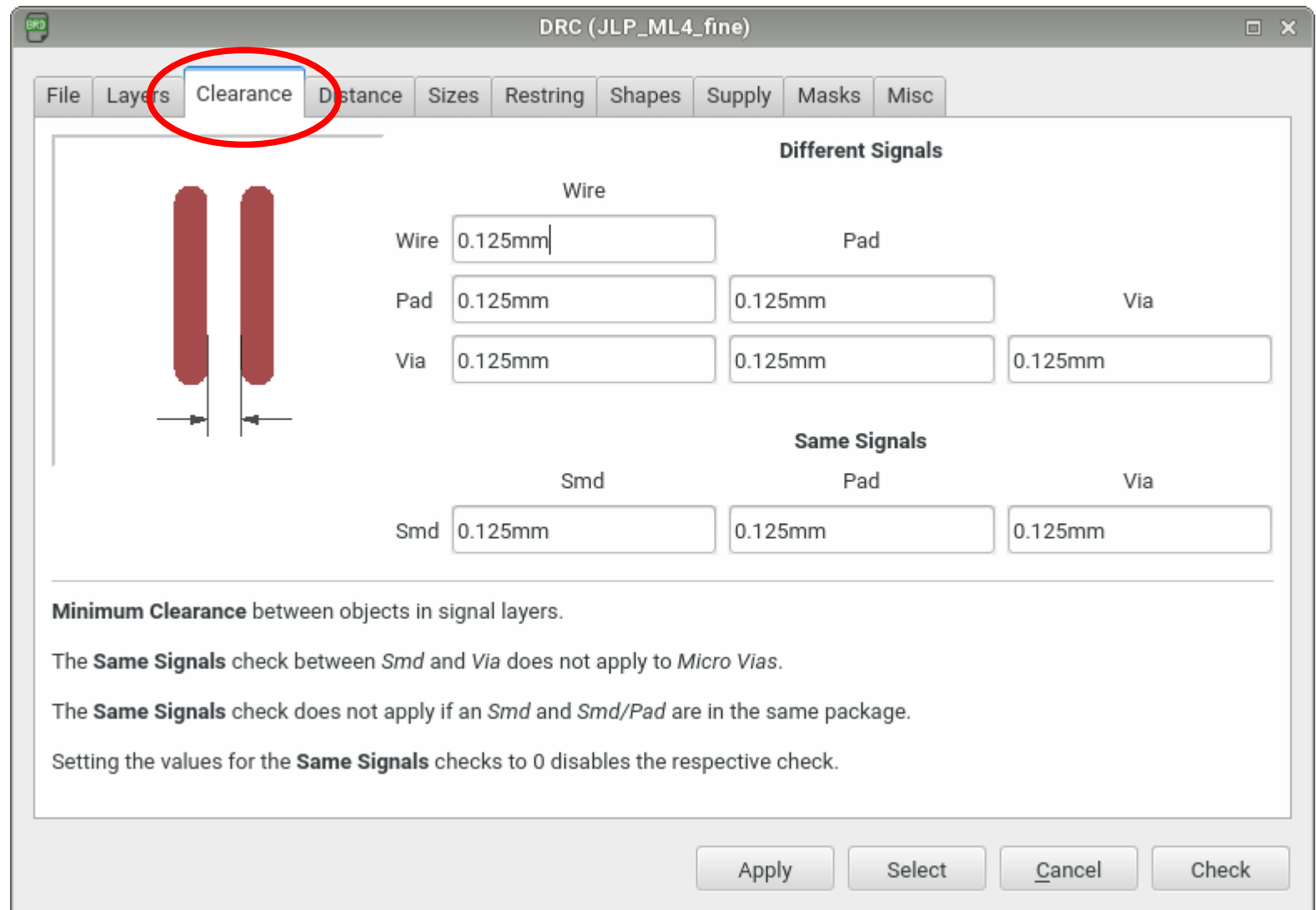
Befehl
DRC



https://github.com/Blunk-electronic/lbr_eagle/tree/master/dru

DRC #2

Befehl
DRC



DRC (JLP_ML4_fine)

File Layers **Clearance** Distance Sizes Restrung Shapes Supply Masks Misc

Different Signals

	Wire	Pad	Via
Wire	0.125mm		
Pad	0.125mm	0.125mm	
Via	0.125mm	0.125mm	0.125mm

Same Signals

	Smd	Pad	Via
Smd	0.125mm	0.125mm	0.125mm

Minimum Clearance between objects in signal layers.

The **Same Signals** check between *Smd* and *Via* does not apply to *Micro Vias*.

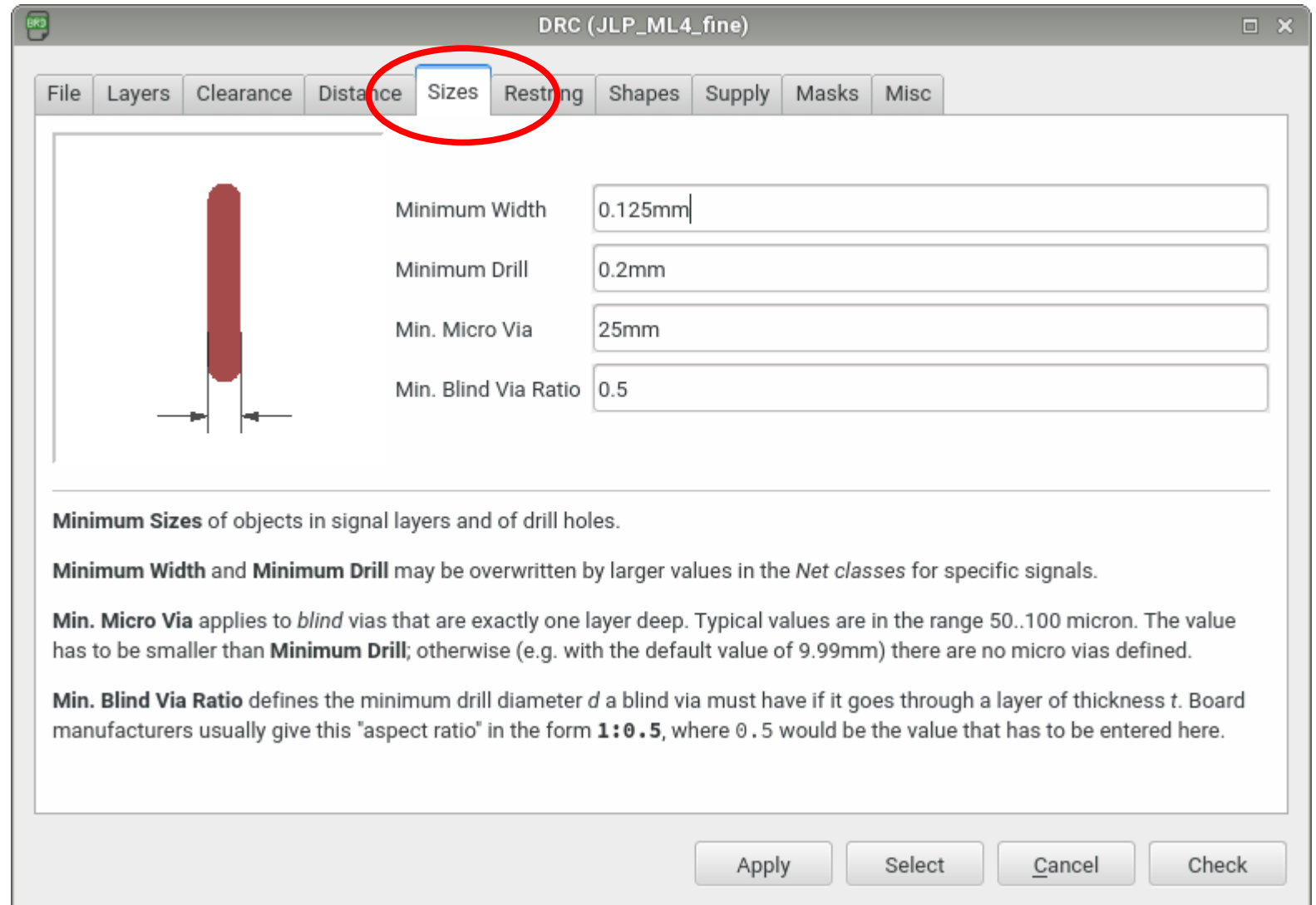
The **Same Signals** check does not apply if an *Smd* and *Smd/Pad* are in the same package.

Setting the values for the **Same Signals** checks to 0 disables the respective check.

Apply Select Cancel Check

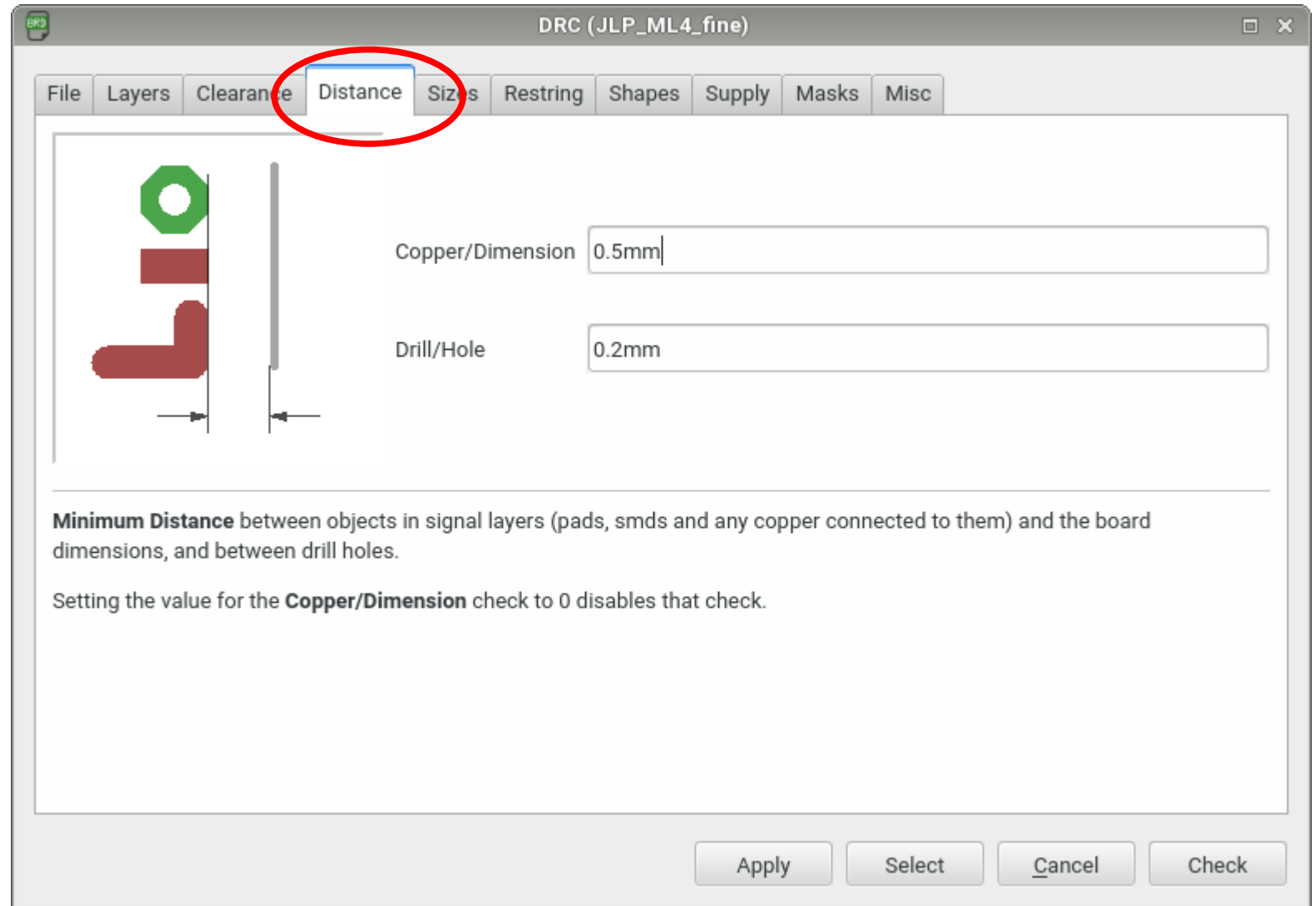
DRC #3

Befehl
DRC



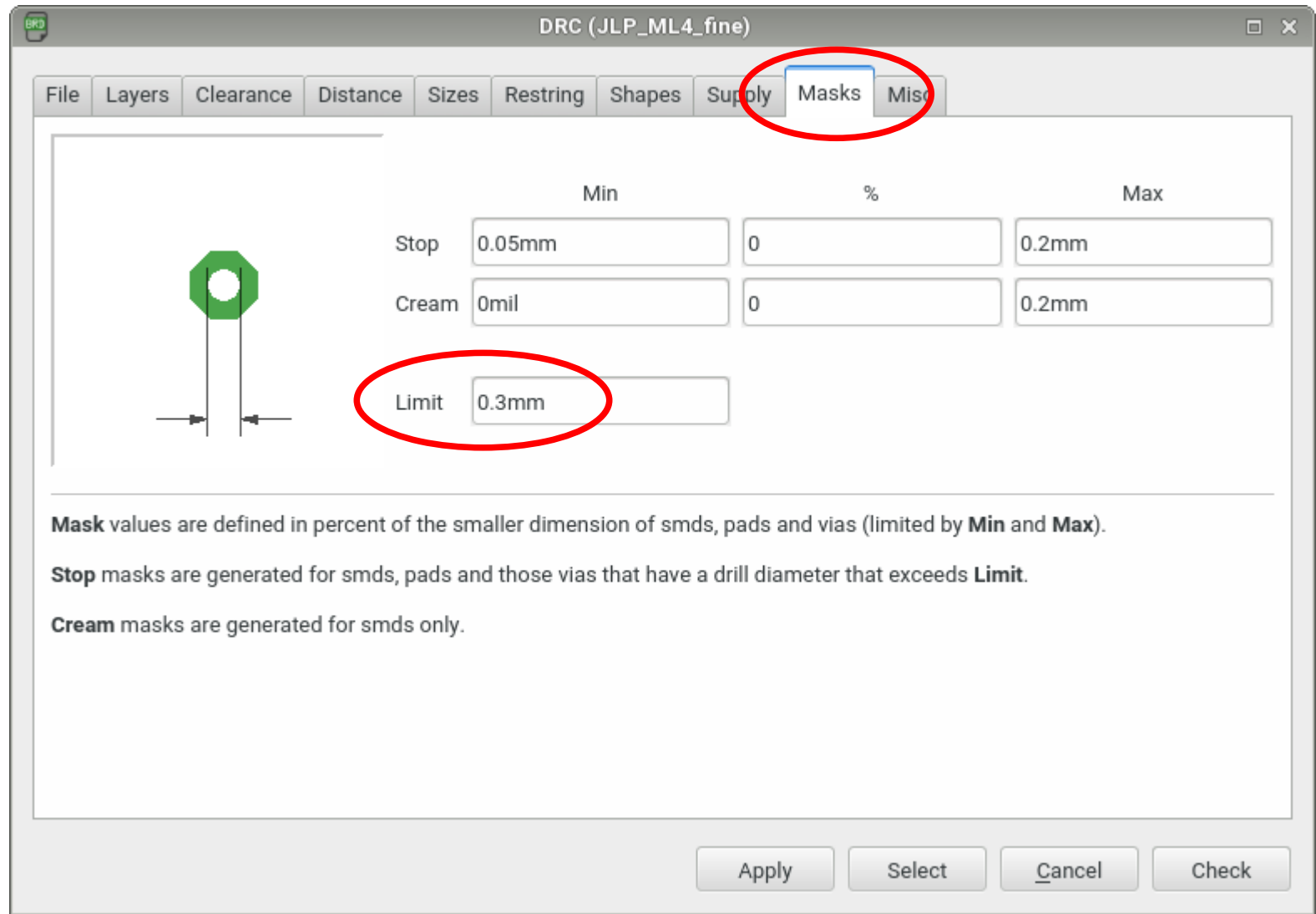
DRC #4

Befehl
DRC



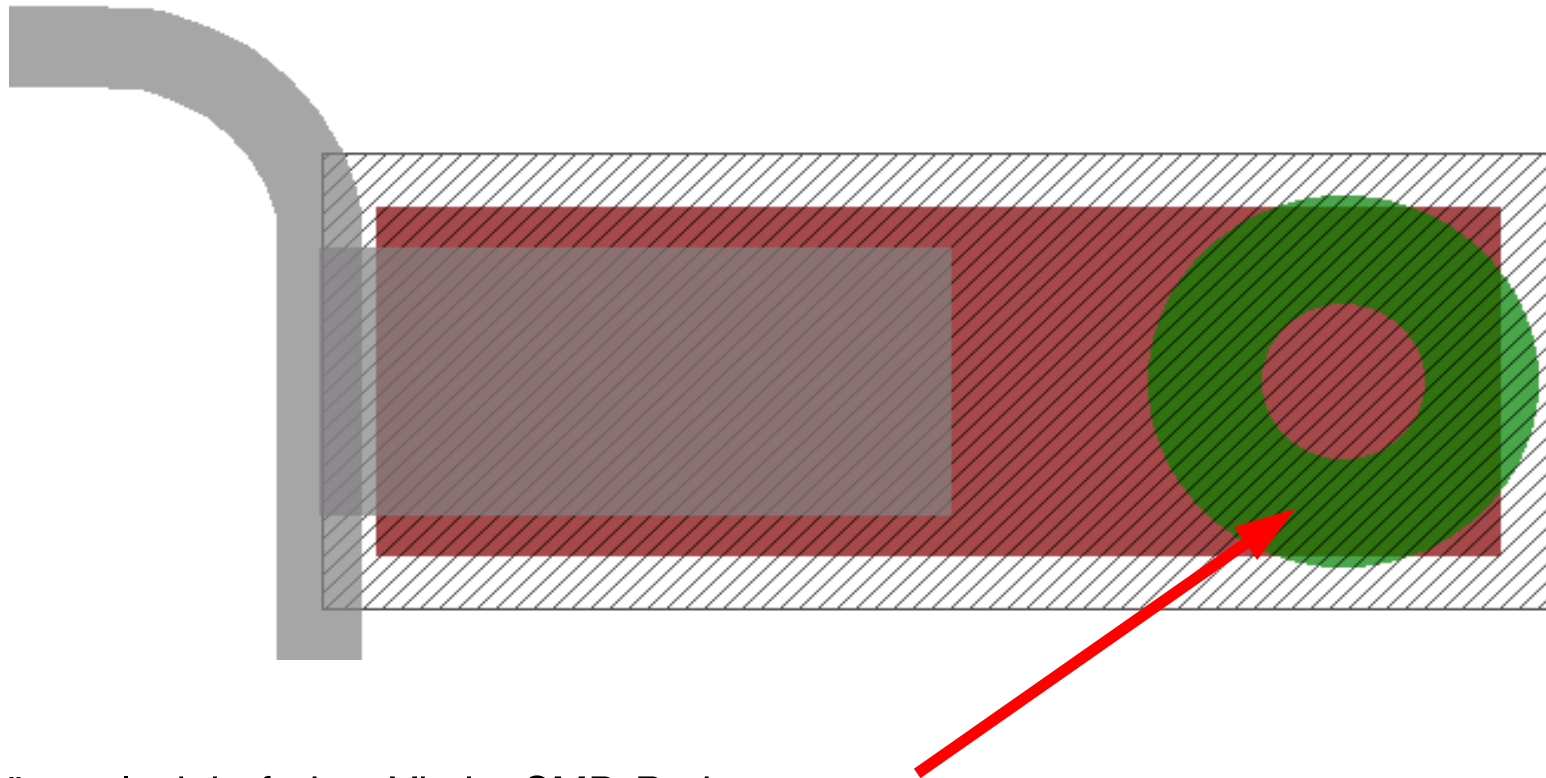
DRC #5

Befehl
DRC



Via-Bohrungen größer 0,3mm ohne Lötstoplack !

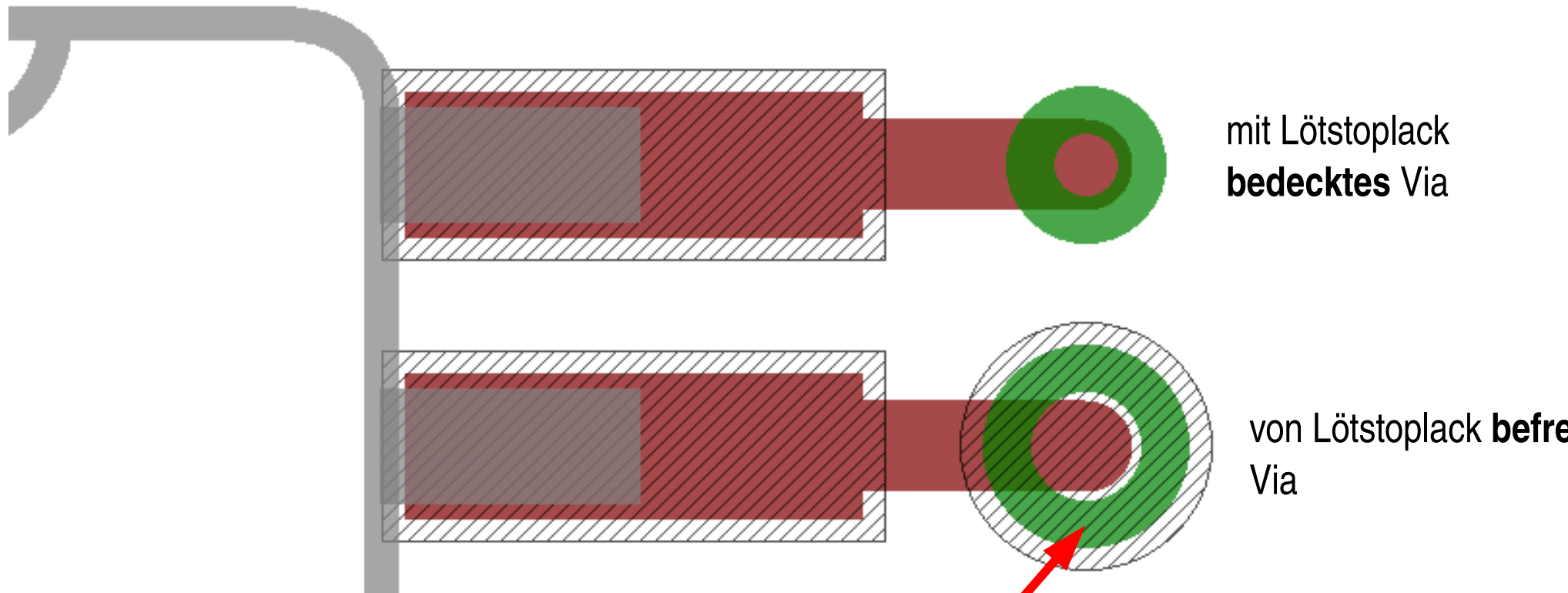
DRC #6



von Lötstoplack befreites Via im SMD-Pad

- ACHTUNG:
- DRC-Einstellung Clearance/Same Signals SMD-Via=0 nötig !
 - **PCB-Bestücker kontaktieren ! Lotpaste kann in Bohrung abfließen !**

Lötstopplack vs. Vias

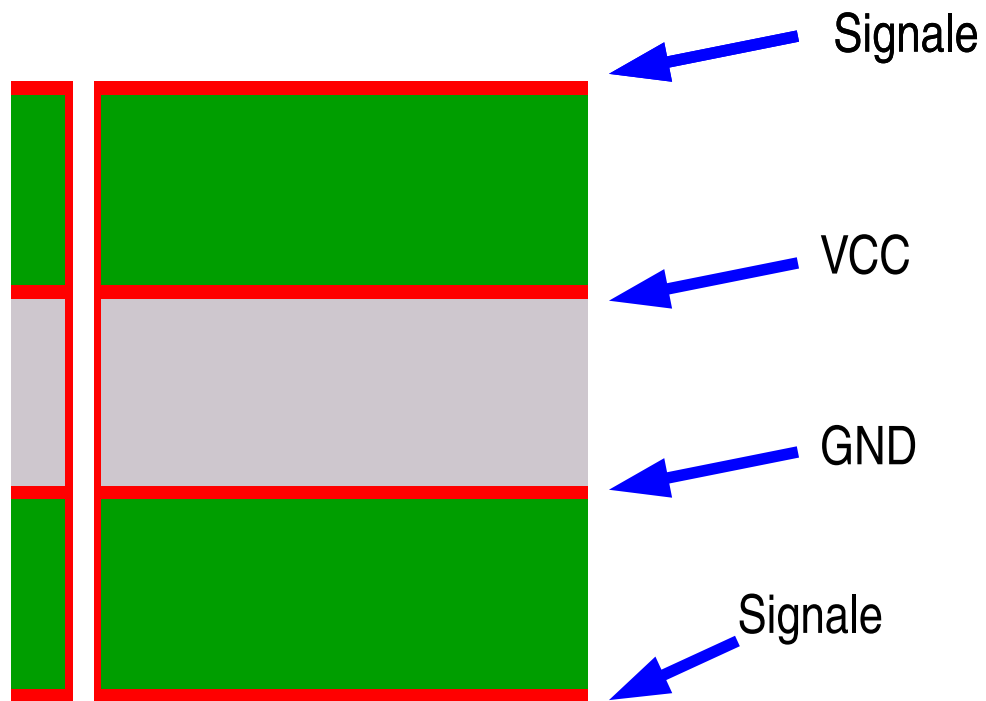


Nicht als Testpunkt für ICT oder FPT
geeignet ! PCB-Bestücker kontaktieren !

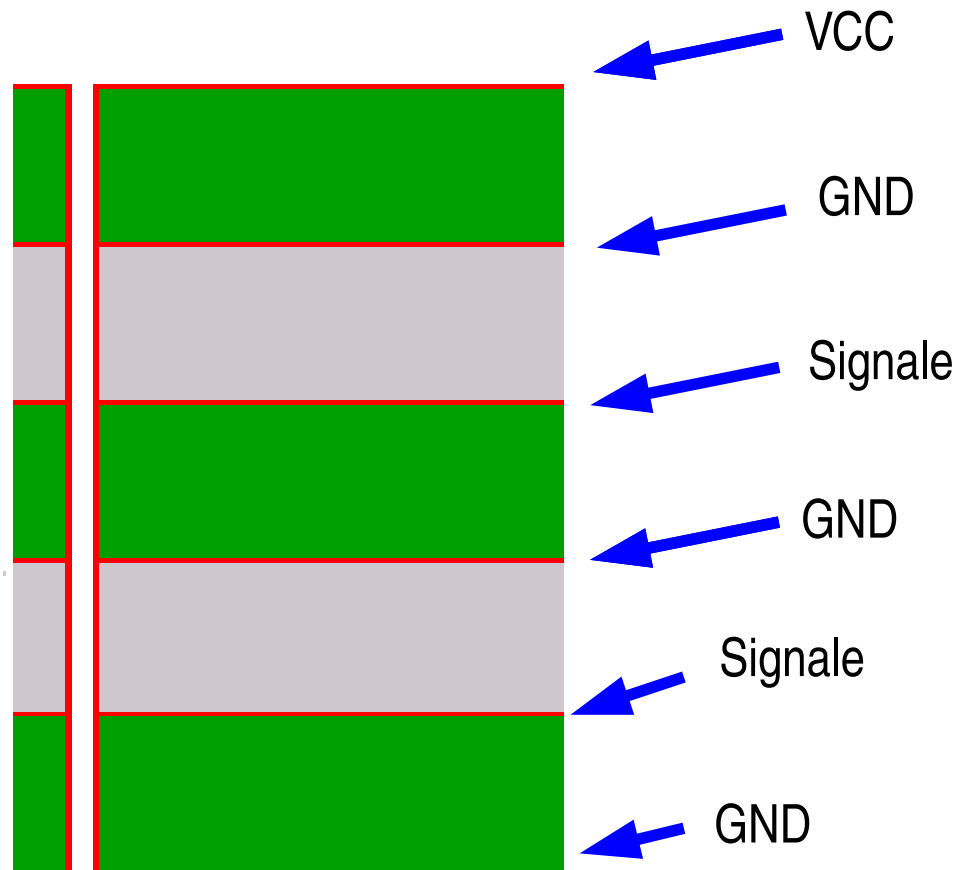
Multilayer PCBs

1. Bedarf Multilayer PCB ?
2. Platzierung Versorgungs/Signallagen ?
3. Layer Setup
4. Vias
5. **Hersteller kontaktieren !**

Lagenplatzierung #1



Lagenplatzierung #2



Layer Setup #1

Befehl DRC

Prepreg

Kern

Nr	Copper	Isolation
1	0.035mm	0.2mm
2	0.035mm	1mm
15	0.035mm	0.2mm
16	0.035mm	

Total: 1.54mm

Setup: $(1+2*15+16)$

Layers are combined through either *core* or *prepreg* material. **a*b** combines layers *a* and *b* with a *core*, while **a+b** does the same with *prepreg*.

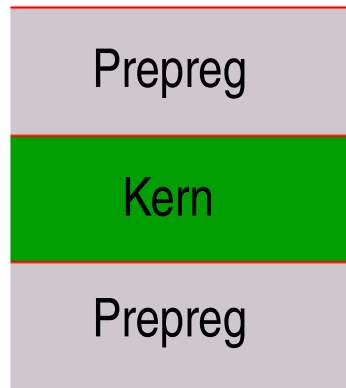
Buried and **through** vias are defined by writing (...).

Blind vias are defined by writing [**t**:...:**b**], which defines a blind via from top to layer *t* and from bottom to layer *b*.

Example: [2: (1+(2*3)+(14*15)+16):15] is a multilayer setup with two cores, combining layers 2/3 and 14/15, respectively, with buried vias going through both cores. The cores are combined through a prepreg and buried vias are produced through the resulting stack. Finally layers 1 and 16 are added, with blind vias going from layer 1 to 2 and layer 15 to 16.

Apply Select Cancel Check

Layer Setup #2



- 4 Lagen
- 1 x Kern
- 2 x Prepreg

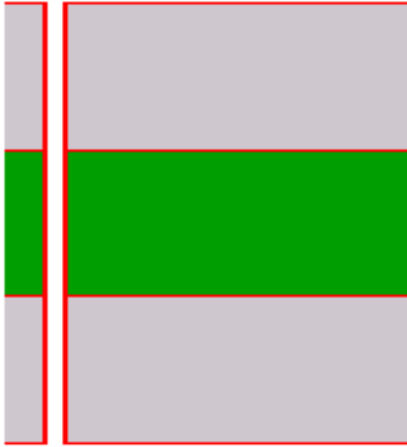
$$1+2*15+16$$



- 6 Lagen
- 2 x Kern
- 3 x Prepreg

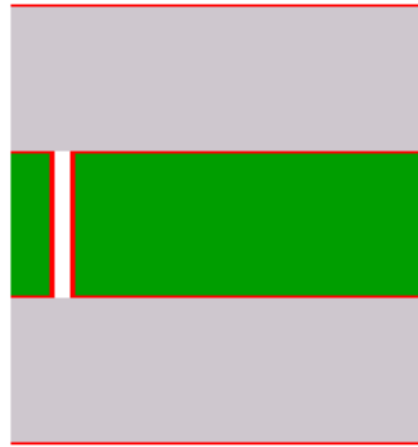
$$1+2*3+14*15+16$$

Vias



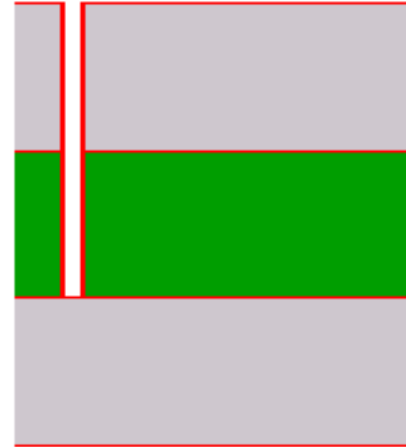
through (durchgehend)

$$(1+2*15+16)$$



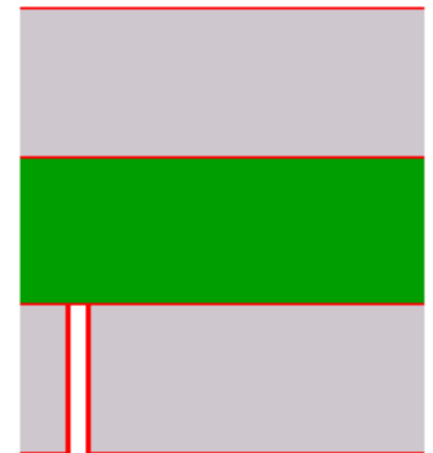
buried
(vergraben)

$$1+(2*15)+16$$



blind
(Sackloch)

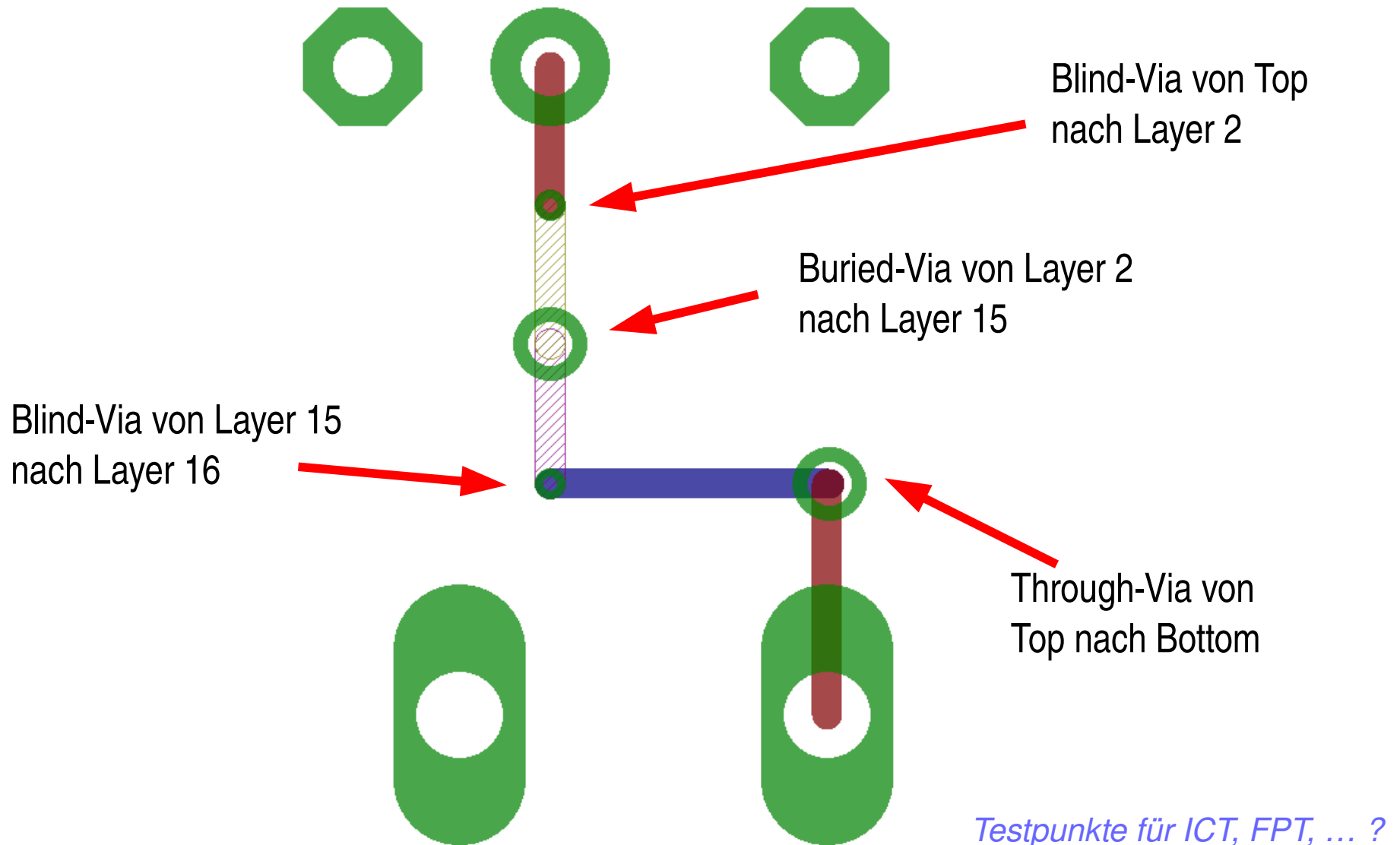
$$[15:1+2*15+16]$$



micro
(nur von außen zur
nächsten Lage)

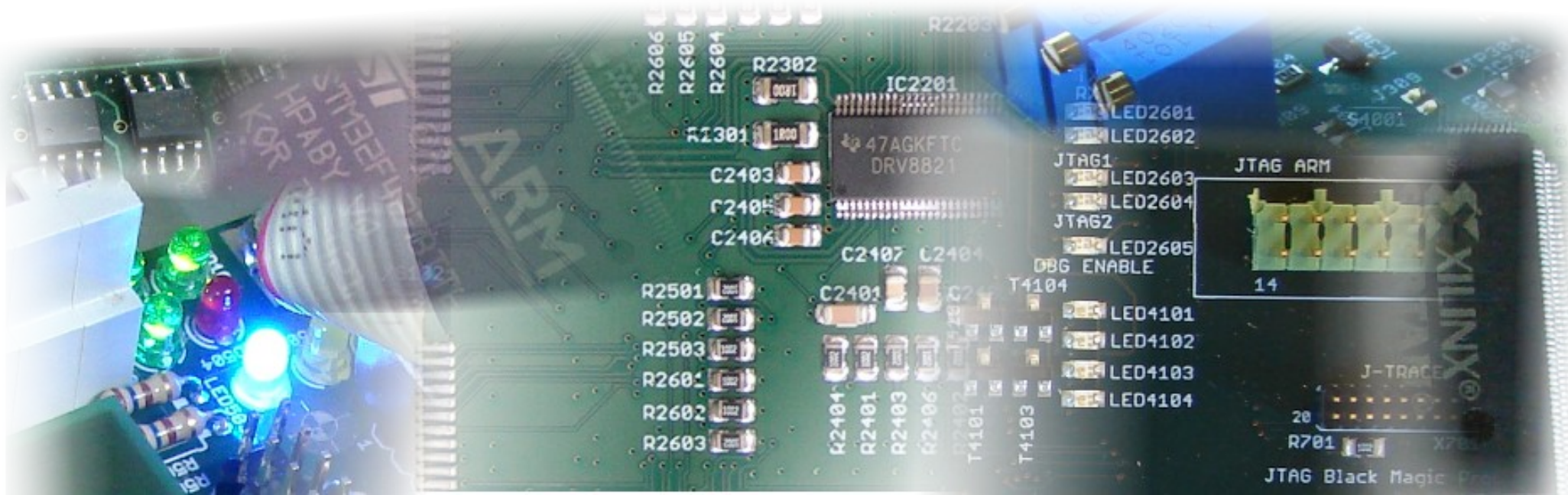
$$[1+2*15+16:15]$$

Routen von Innenlagen





http://www.blunk-electronic.de/pdf/Design_Checklist_en.pdf



Dokumentation #1

Layer 21/22 und 51/52

Befehle:

SMASH,

MOVE,

GROUP,

CHANGE

- **SIZE**

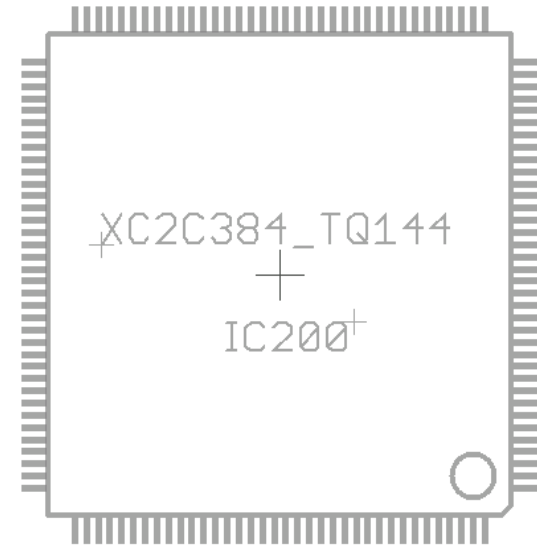
- **RATIO**

vorher:

C310



100n

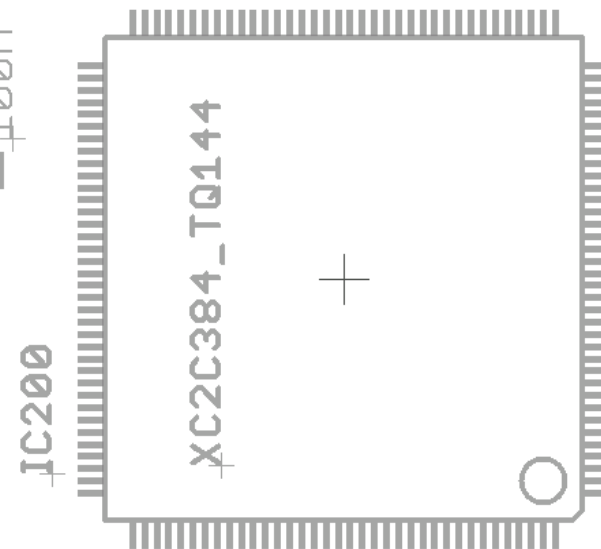


nachher:

C310



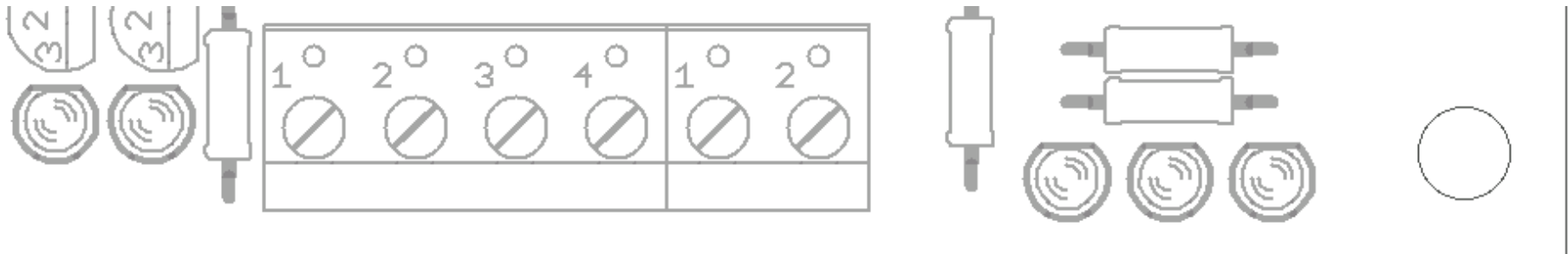
100n



Dokumentation #2

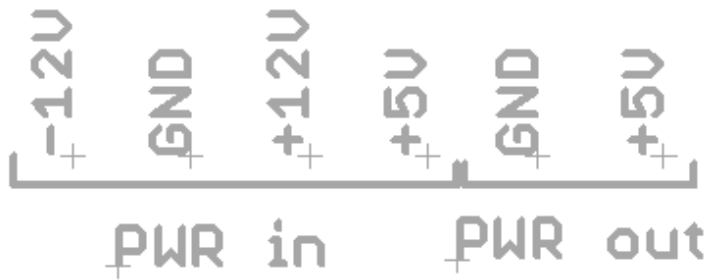
Layer 51/52 (tDocu / bDocu)

Befehle: **TEXT**, **WIRE**, **MOVE**, **GROUP**,
CHANGE TEXT / SIZE / RATIO



P10_A1 (blue)

P10_A0 (blue)



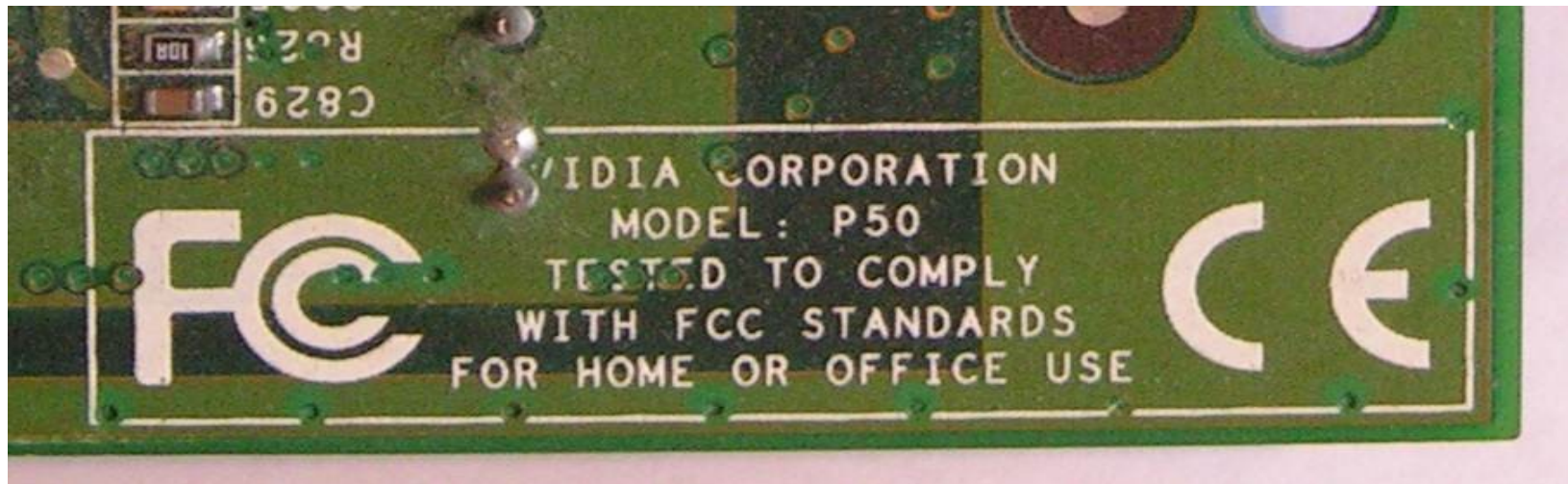
+12V (green)

+5V (green)

-12V (green)

Dokumentation #3

Layer 21/22 (tPlace / bPlace)

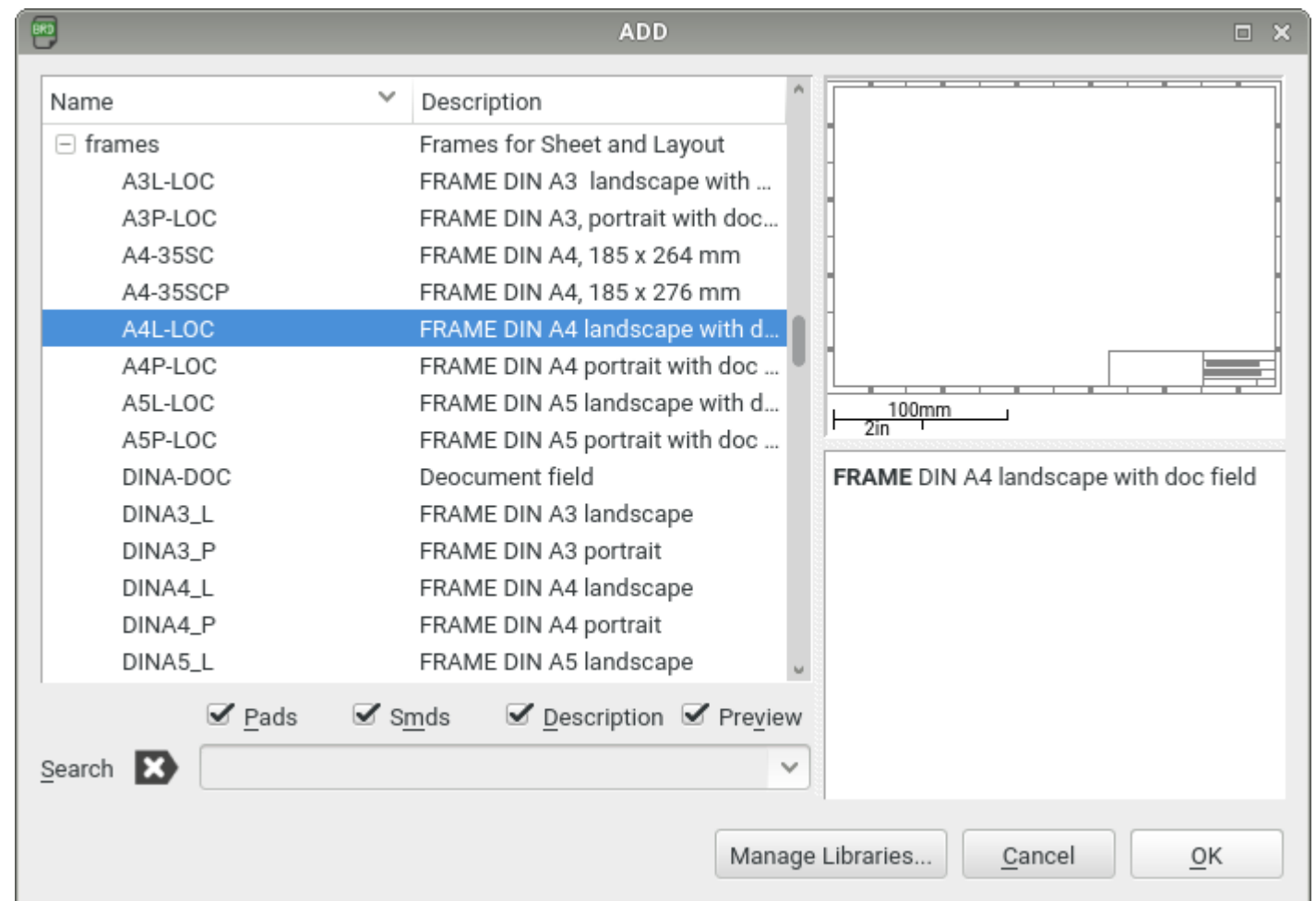


Dokumentation #4

Zeichnungsrahmen

Layer 48 (Document)

Befehle:
ADD,
MOVE,
GROUP



Materialliste, Bestückliste, & Netzliste ...

Datei/Export/Import/...

RUN bom

RUN export-ict-netlist-pad-coordinates

RUN ipc-d-356

RUN statistic-brd

- **Bestückungsvarianten**
- **Export aus BRD/SCH**
- **Sonderzeichen**

Bibliothek Aufbau #1

The screenshot shows the EAGLE 8.2.2 free software interface. The left pane displays a library browser with a tree view under 'Libraries' and 'Managed Libraries'. The '74xx-eu.lbr' library is expanded, and the '74*06' component is selected and highlighted with a red circle. The right pane shows the details for the '74*06' component, including its description, logic symbol, physical package drawing, and a table of device variants.

74*06 Hex INVERTER, open collector high-voltage output

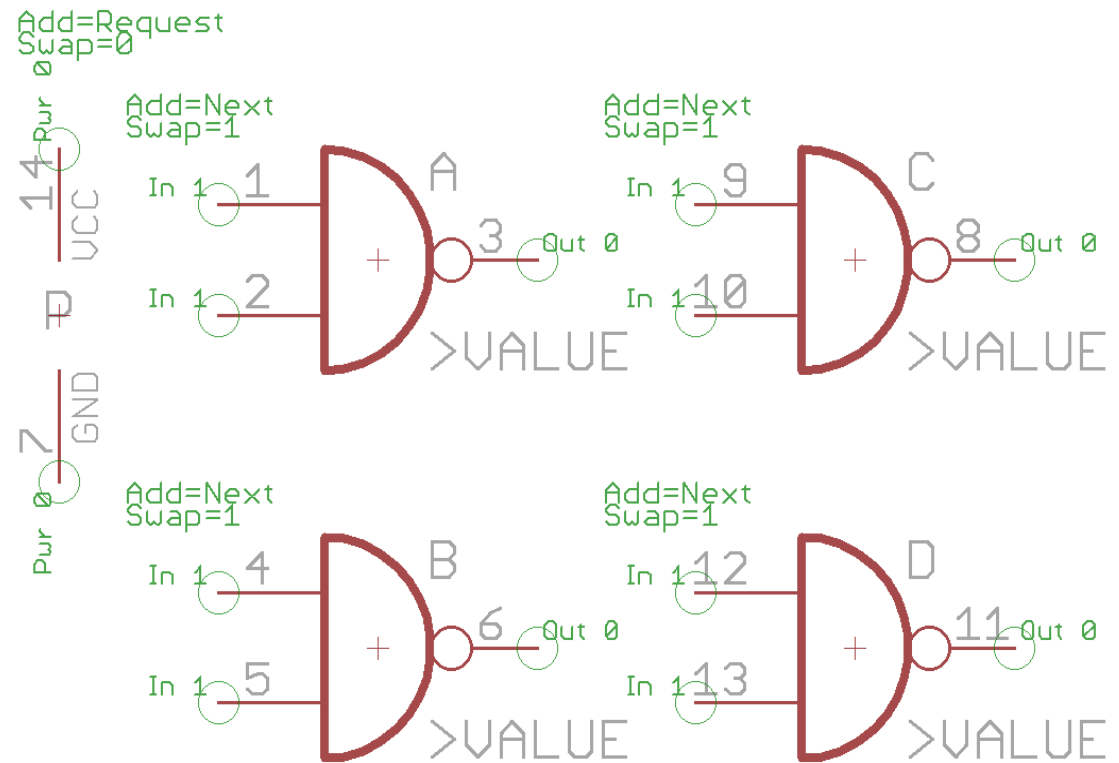
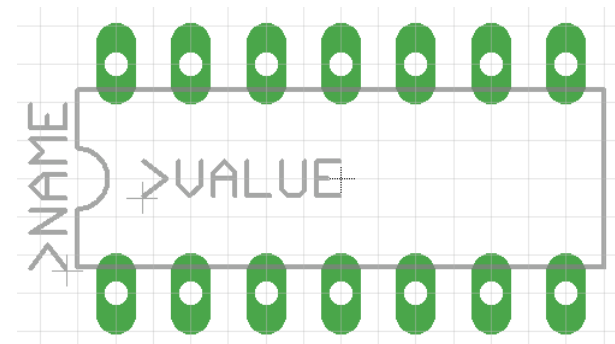
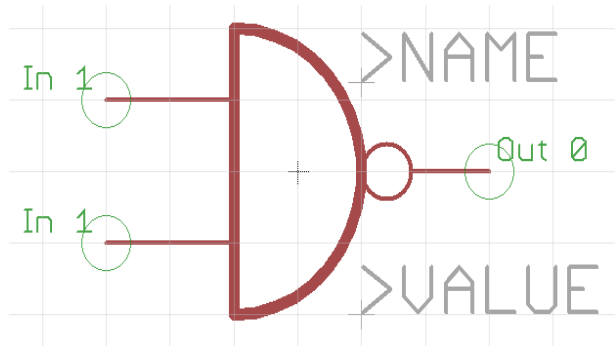
74xx-eu.lbr

Hex INVERTER, open collector high-voltage output

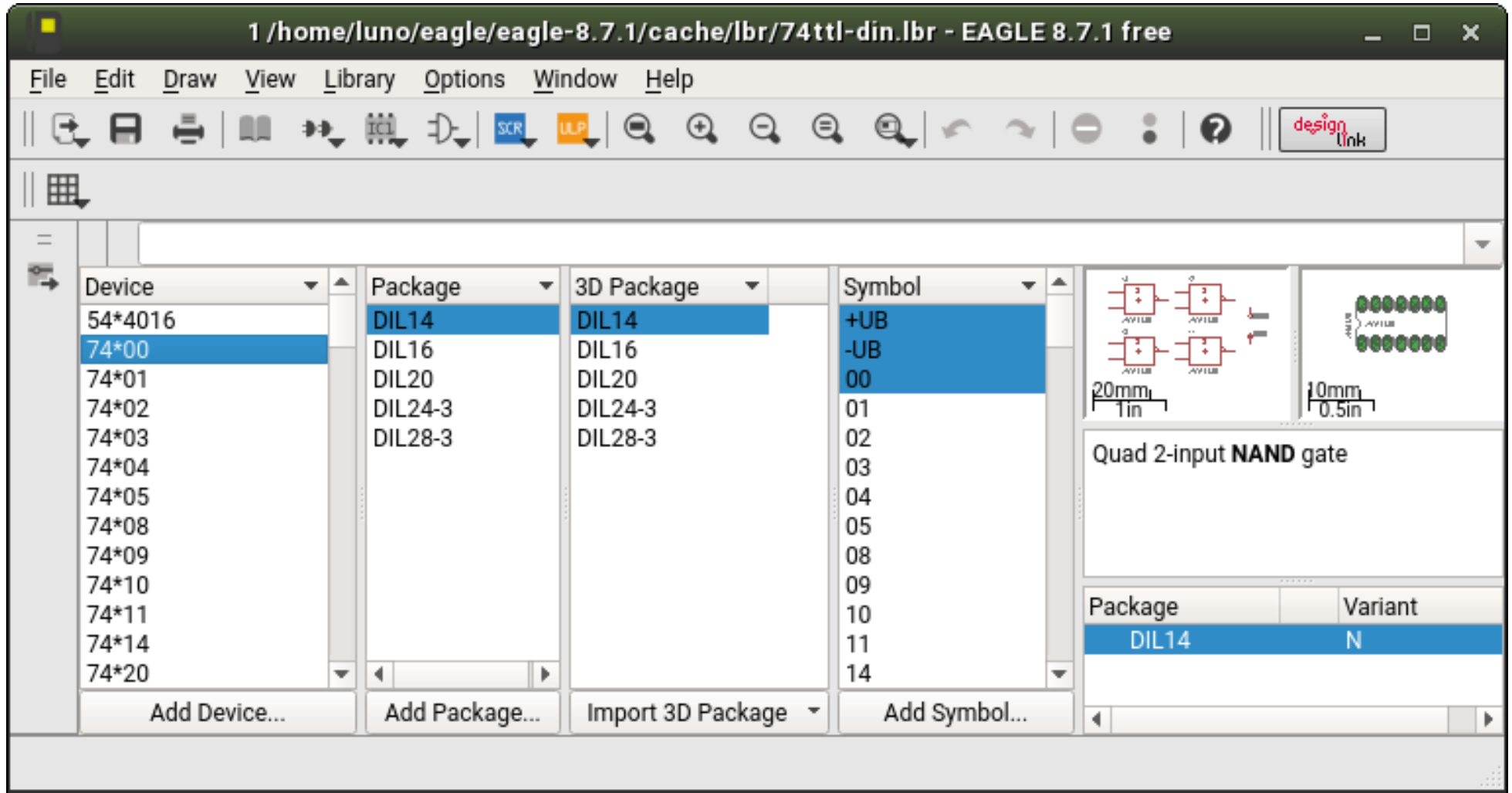
Small Outline package 150 mil

Device	Package Description
74AC06D	SO14 Small Outline package 150 mil
74AC06FK	LCC20 Leadless Chip Carrier Ceramic Package
74AC06N	DIL14 Dual In Line Package
74ACT06D	SO14 Small Outline package 150 mil
74ACT06FK	LCC20 Leadless Chip Carrier Ceramic Package
74ACT06N	DIL14 Dual In Line Package
74LS06D	SO14 Small Outline package 150 mil
74LS06FK	LCC20 Leadless Chip Carrier Ceramic Package

Bibliothek Aufbau #2



Bibliothek Aufbau #3



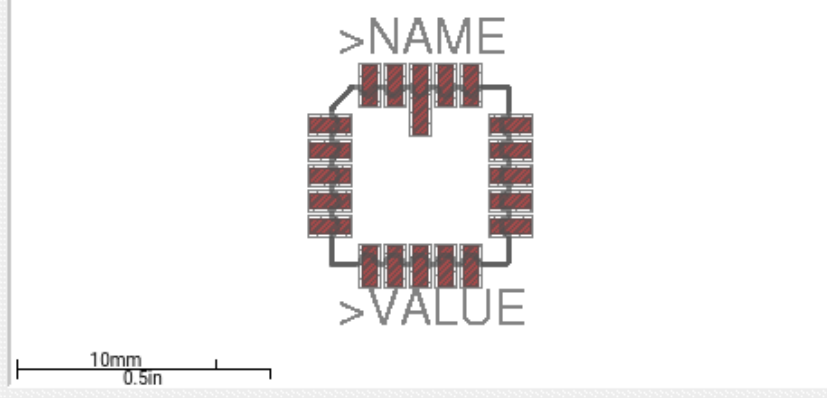
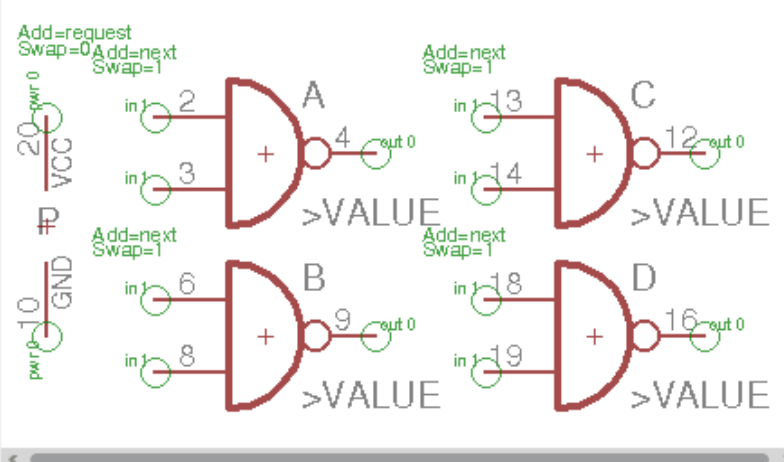
https://github.com/Blunk-electronic/lbr_eagle

Bibliothek Aufbau #4

1 Library - /home/luno/eagle/eagle-8.2.2/cache/lbr/74xx-eu.lbr (74*00.dev) - EAGLE 8.2.2 free

File Edit Draw View Library Options Window Help

0.1 inch (2.1 0.4)



Description

Quad 2-input NAND gate

Technologies	Attributes
7400FK	
74AC00FK	
74ACT00FK	
74ALS00FK	
74AS00FK	
74HC00FK	
74HCT00FK	
74LS00FK	
74S00FK	

Package	Variant	
DIL14	N	✓
LCC20	FK	✓
SO14	D	✓

New Connect

Prefix IC

Value Off On

◆ Left-click&drag to define group (or left-click to start defining a group polygon)

Symbole bearbeiten

Befehle:

WIRE,

PIN,

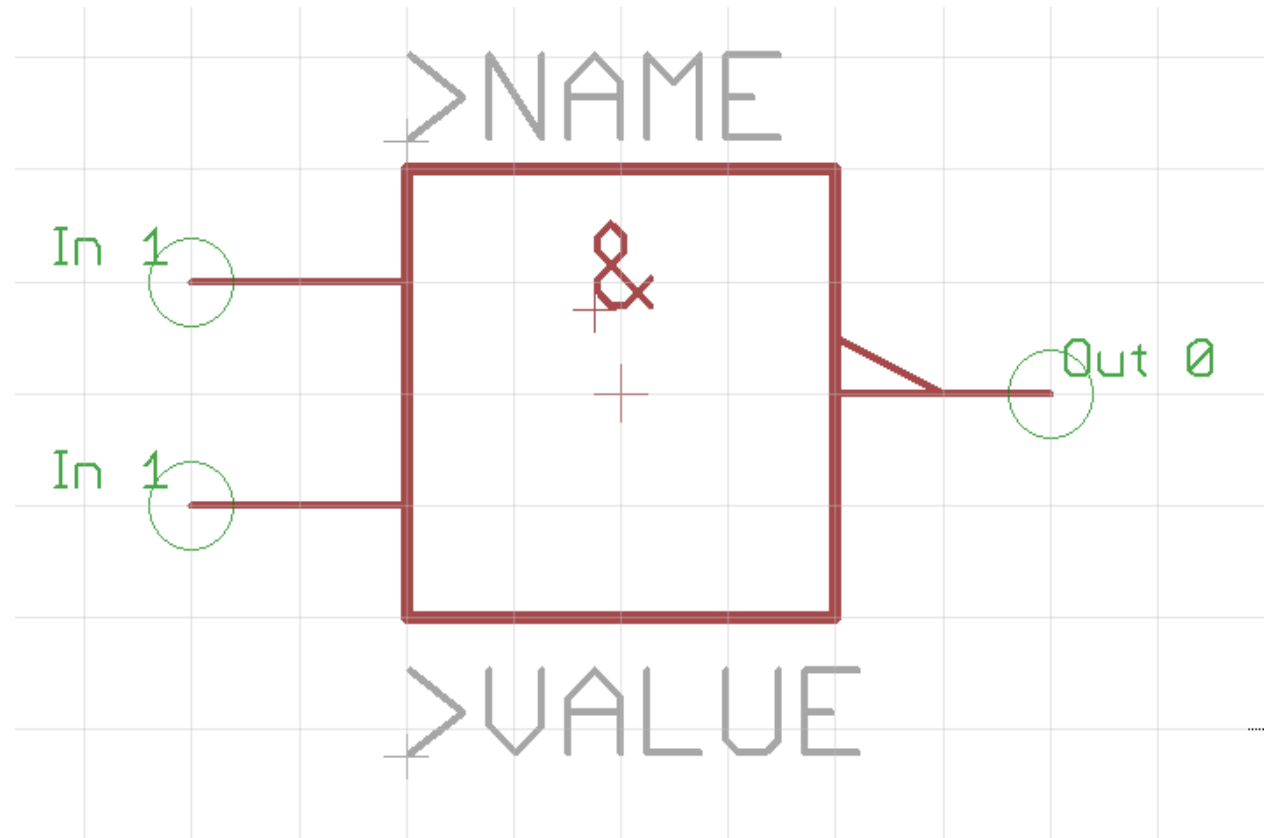
TEXT,

CHANGE

- DIR

- FONT

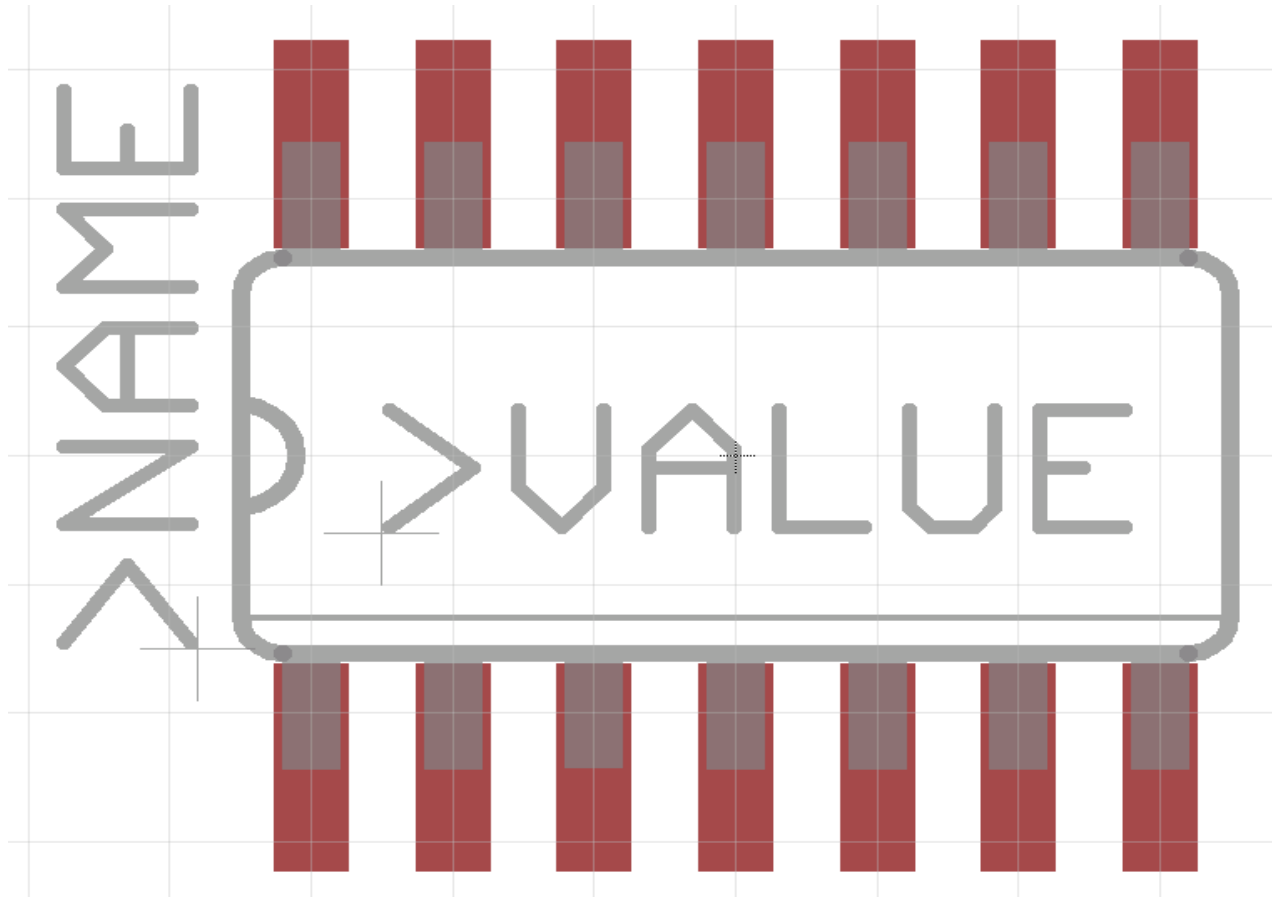
- SIZE



Gehäuse bearbeiten

Befehle:

**LAYER,
PAD,
SMD,
WIRE,
MOVE,
GROUP,
DEL,
NAME,
CHANGE**



Device anlegen

Befehle: **ADD**, **PAC**, **CON**, **PRE**, **ATTR**, **VAL ON/OFF**

Description
Quad 2-input **NAND** gate

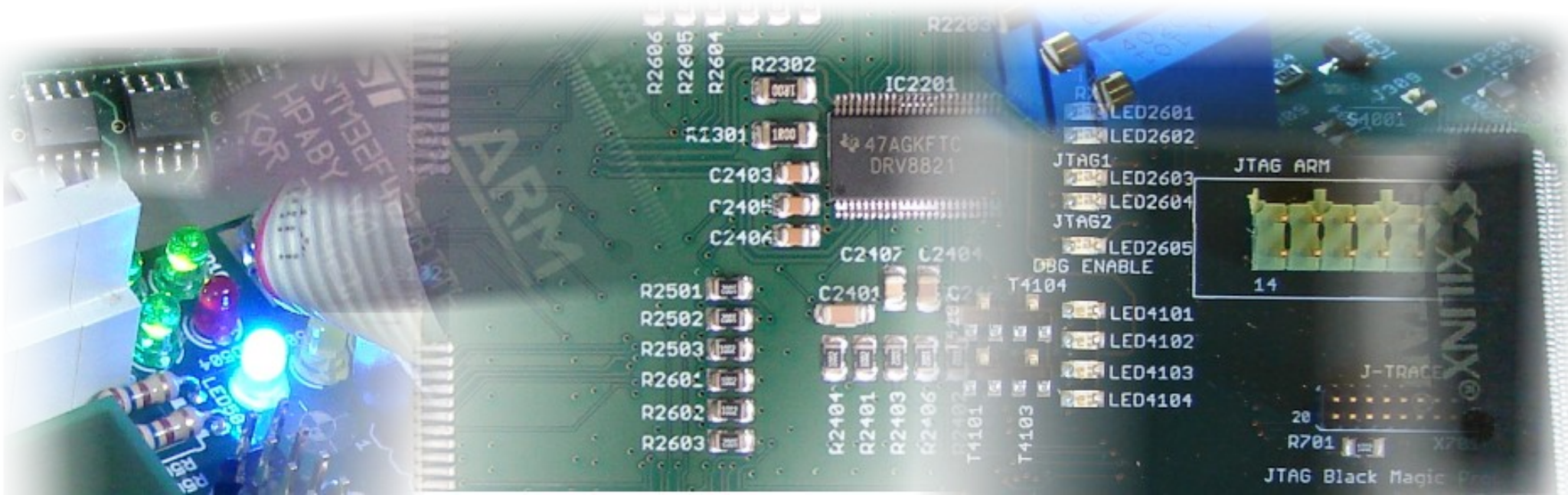
Technologies	Attributes
7400FK	
74AC00FK	
74ACT00FK	
74ALS00FK	
74AS00FK	
74HC00FK	
74HCT00FK	
74LS00FK	
74S00FK	

Package	Variant	
DIL14	N	✓
LCC20	FK	✓
SO14	D	✓

New Connect
Prefix IC
Value Off On



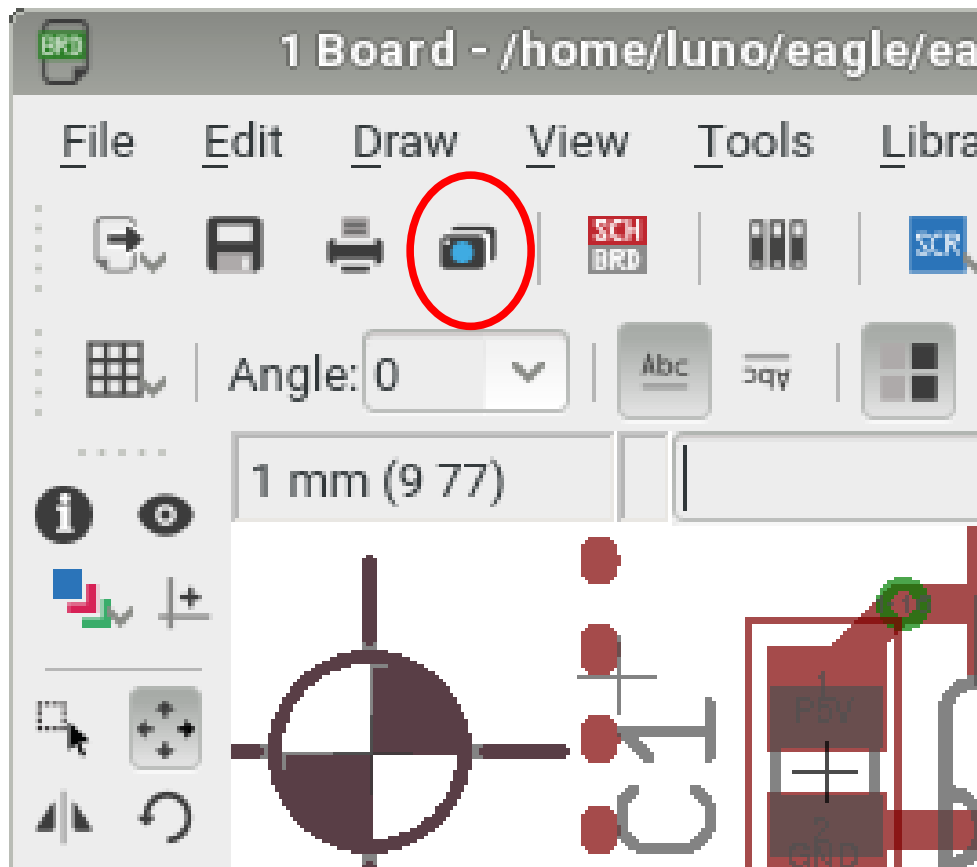
http://www.blunk-electronic.de/pdf/library_tutorial.pdf



CAM-Prozessor #1

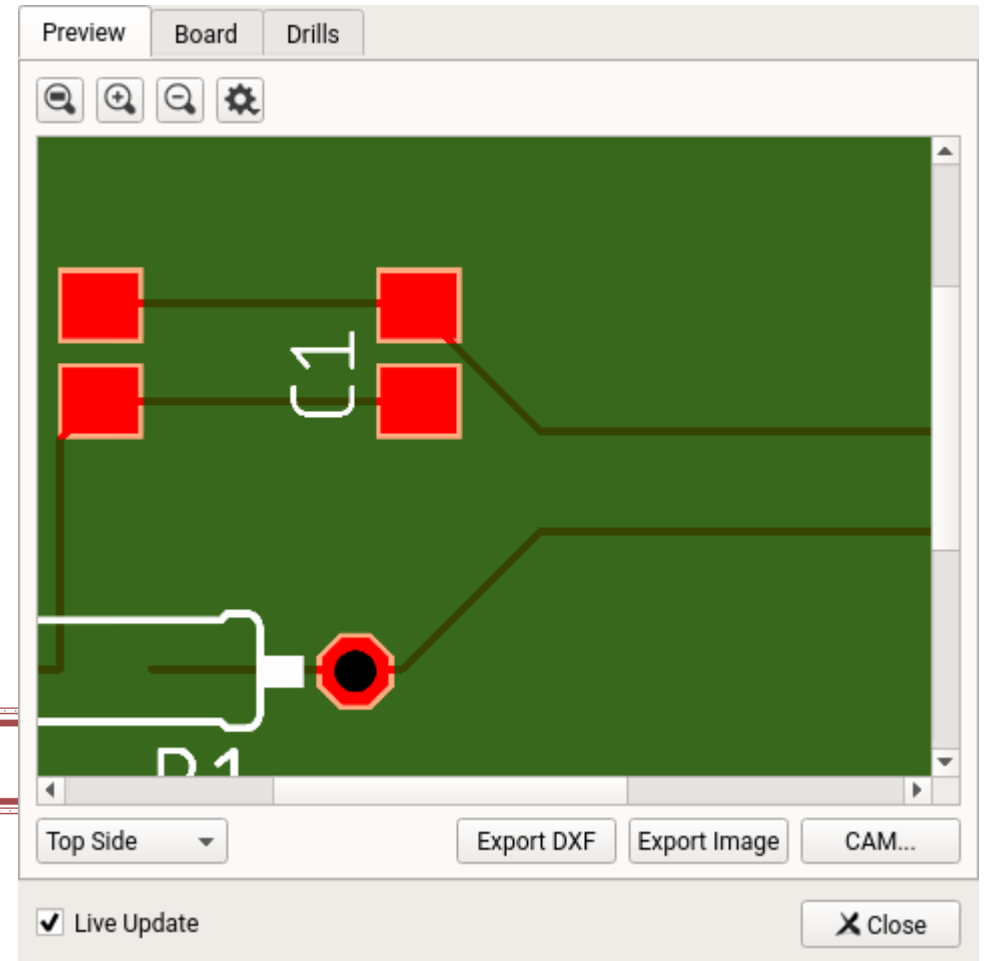
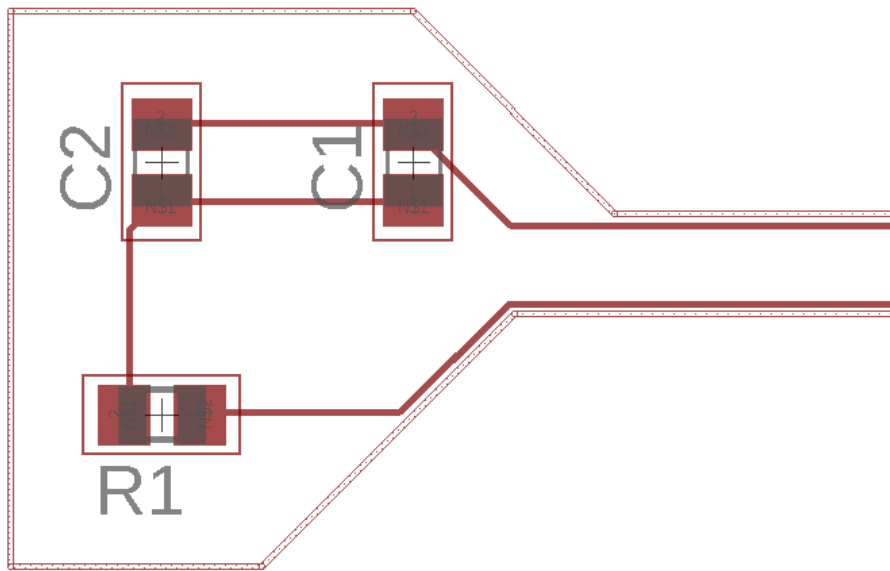


1. Designdaten bleiben beim Entwickler !
2. Sende niemals Designdaten an einen PCB-Hersteller !
3. Sende niemals Designdaten an einen PCB-Bestücker !



CAM-Prozessor #2

Plot- und
Bohrdaten
Voransicht



CAM-Prozessor #3

Statistiken



Preview Board Drills

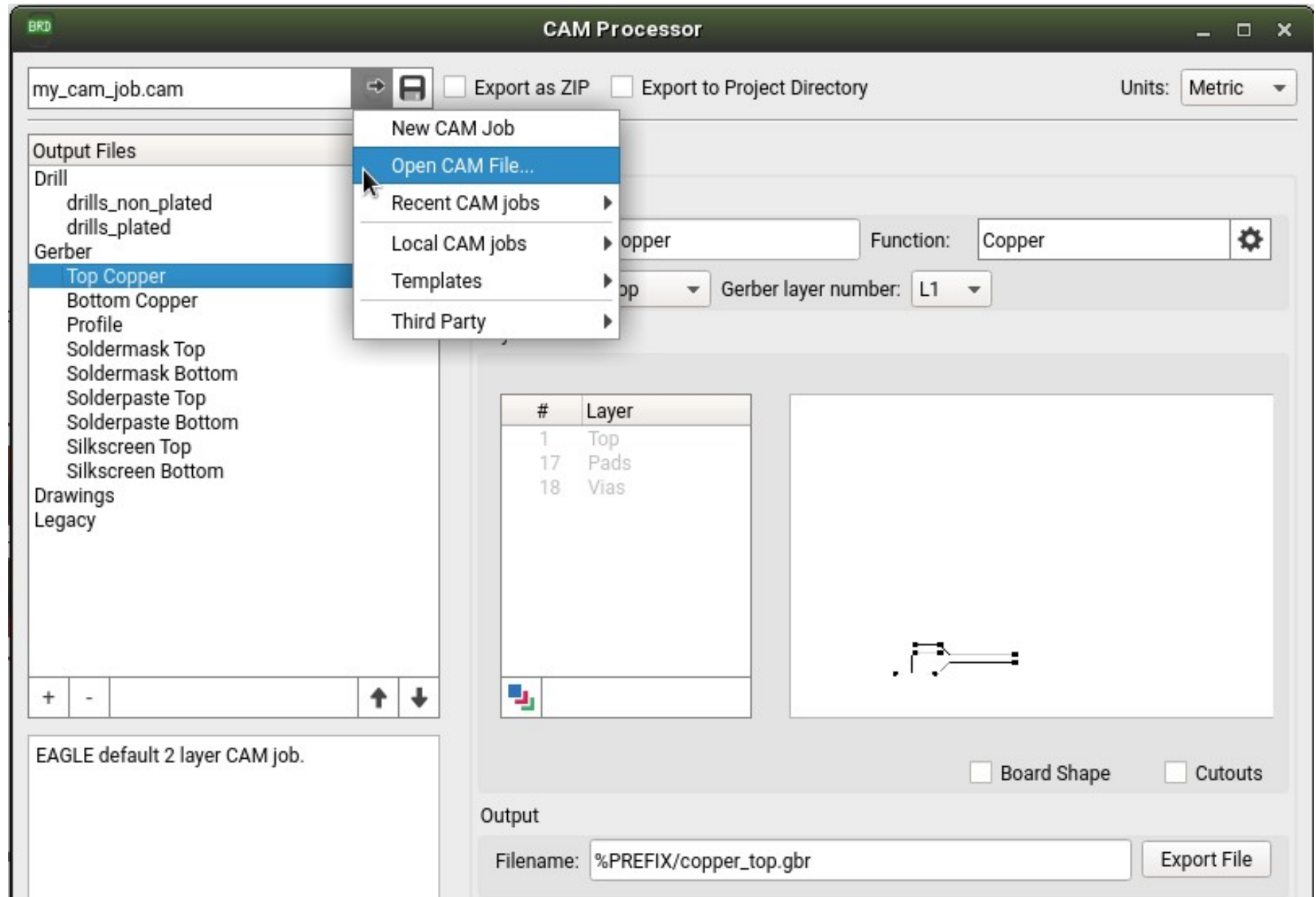
Property

- ▶ Board
- ▼ Stackup
 - Copper Layers 2
 - Board Thickness 1.57mm 0.062in
- ▼ Components
 - Components on Top Layer 4
 - Components on Bottom Layer 0
 - SMD Components on Top Layer 3
 - SMD Components on Bottom Layer 0
 - PTH Components on Top Layer 1
 - PTH Components on Bottom Layer 0
 - Component Density Top Layer 0.64cm-2 4.10in-2
 - Component Density Bottom Layer 0.00cm-2 0.00in-2
- ▼ Pads
 - SMD Pads Top 6
 - SMD Pads Bottom 0
 - SMD Pad Density Top 0.95cm-2 6.15in-2
 - SMD Pad Density Bottom 0.00cm-2 0.00in-2
- ▶ Drills
- ▼ Routing
 - Number of Signals 3
 - Minimum Copper Trace Width 0.15mm 0.006in

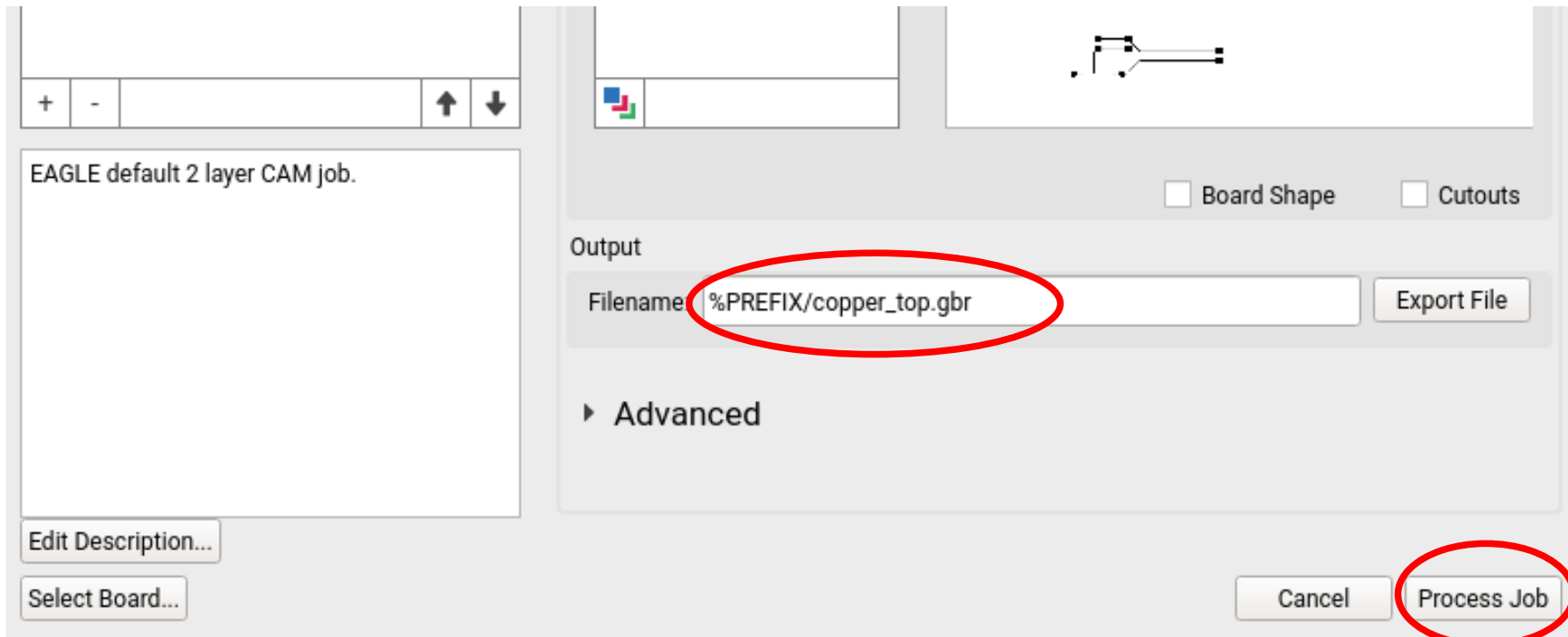
Live Update Close

Reduziere Vielfalt !

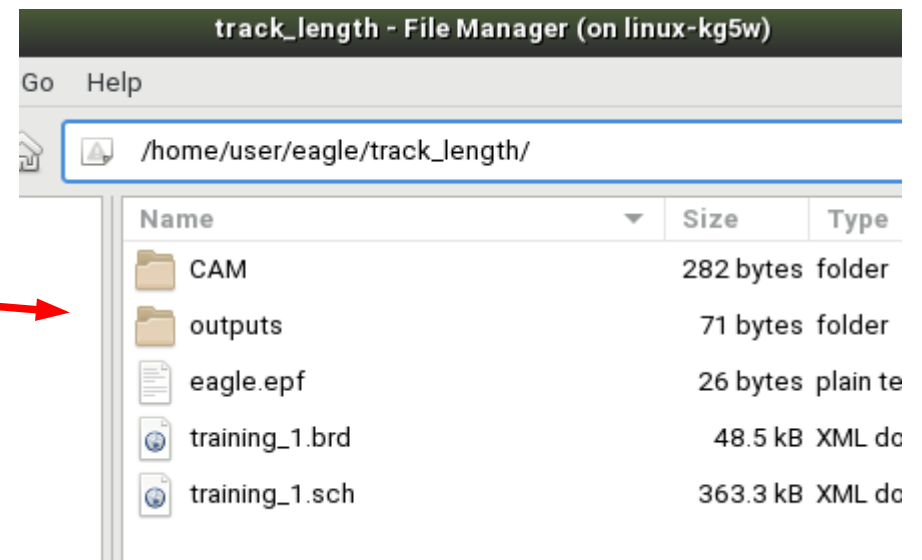
CAM-Prozessor #4



CAM-Prozessor #5

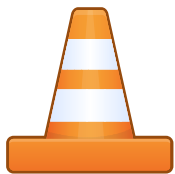


CAM-Daten liegen
anschließend hier



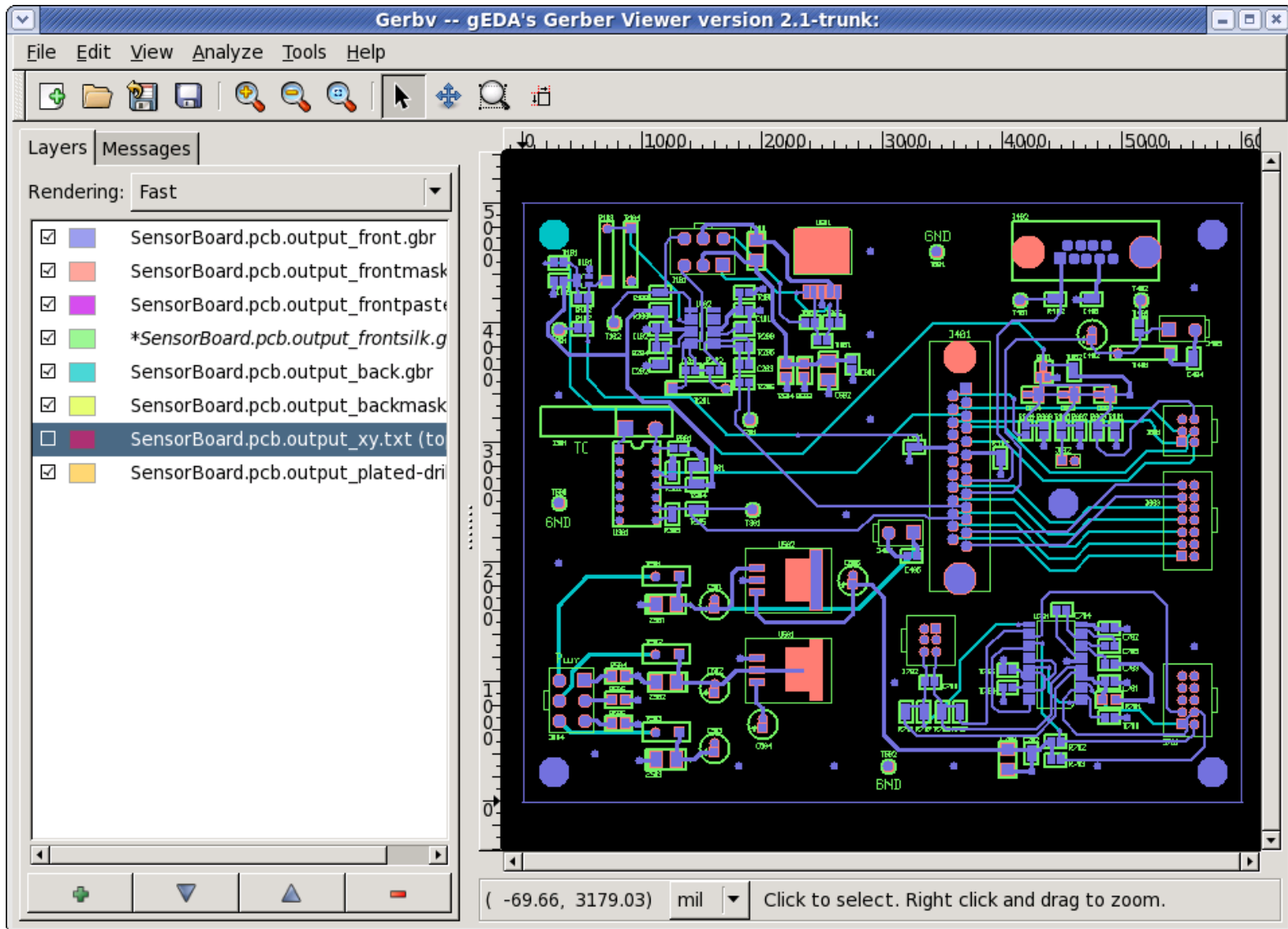
CAM-Prozessor #6

Änderungen in
Datei **eagle.def**
(Version 7.x)



```
[EXCELLON]
Type    = DrillStation
Long    = "Excellon drill station, coordinate format 2.5 inch"
Init    = "%%\nM48\nM72\n"
Reset   = "M30\n"
ResX    = 10000
ResY    = 10000
;Rack   = ""
DrillSize = "%sC%0.5f\n"      ; (Tool code, tool size)
AutoDrill = "T%02d"          ; (Tool number)
FirstDrill = 1
BeginData = "%%\n"
Units    = Inch
Select   = "%s\n"           ; (Drill code)
Drill    = "X%1.0fY%1.0f\n" ; (x, y)
Info     = "Drill File Info:\n"
          "\n"
          " Data Mode      : Absolute\n"
          " Units              : 1/10000 Inch\n"
          "\n"
```

Gerbv

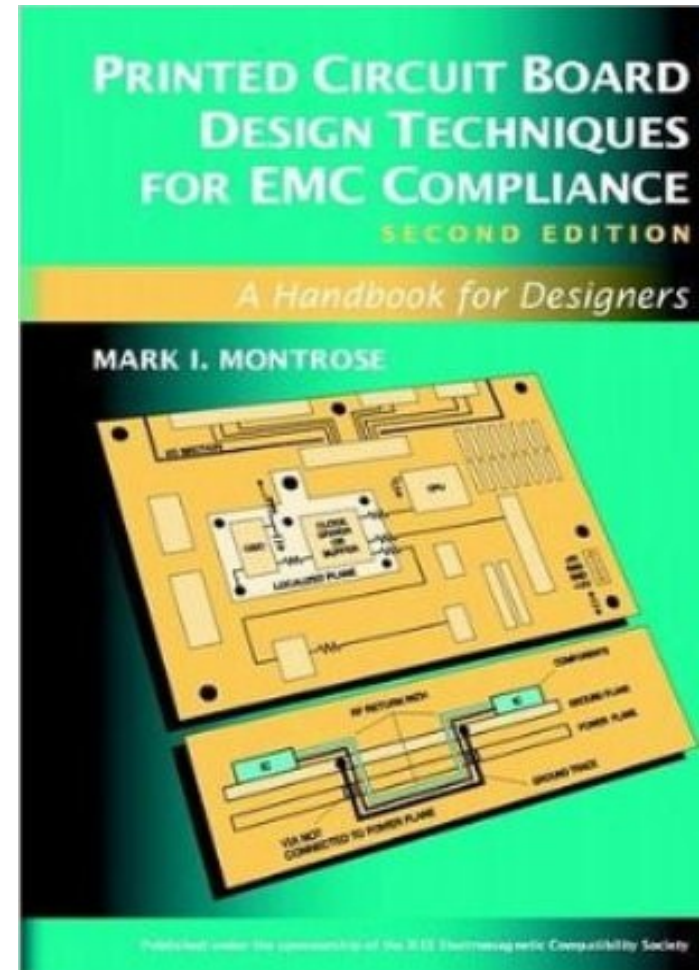


<http://gerbv.geda-project.org>

Literatur #1

Printed Circuit Board Design
Techniques for EMC Compliance:
A Handbook for Designers

(IEEE Press Series on Electronics
Technology)



Literatur #2

Joachim Franz
EMV

Störungssicherer Aufbau
elektronischer Schaltungen

ISBN 3-519-10397-4



Links



PCB Herstellung:

www.jlp.de



Bauteile:

www.ax-electronic.de





Danke für Ihre Aufmerksamkeit !

