Blunk electronic
owner: Dipl.-Ing. Mario Blunk
Buchfinkenweg 3
99097 Erfurt / Germany

cellular +49 (0) 176 2904 5855
office phone +49 (0) 361 6022 5184
email mario.blunk@blunk-electronic.de
web www.blunk-electronic.de

VAT ID DE292765719
German Tax ID 151/208/15161

Design Checklist for Electronic Schematics and PCB Layouts

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Abstract: *Guideline and checklist for development and drawing of electronic circuits, schematics and PCB layouts. Focus is on issues critical for system reliability, stability, testability and manufacturing often neglected and rarely covered by text books. Specials regarding the usage of the CAE tool EAGLE[1] Version 6.5.x are also touched.*

Keywords: *device models, PCB, library, ratings, Boundary Scan, JTAG, IEEE1149.1, jumper, designators, values, numbers, net class, placement, alternative fitting, DFT, SMD, THT, reset, power-up, power cycling, FPGA, CPLD, pull resistors, unused pins, floating pins, ESD, vector font, prototype, solder stop lacquer, shorts, track width, temperature, thickness, drill size, connectors, via, pad, reference marks, German, English, translation, DRC, ERC, polygons, airwire, I²C, pull-resistors, dynamic, static, rise/fall time, silk screen, width, Gerber Data, drill, tolerances , slitted hole, slotted hole, millings, plated*

1 EAGLE is a registered trademark of *CadSoft Computer GmbH*.

1 Introduction

By providing this checklist I let my customers participate in my expertise I have been collecting over years as design and test development engineer. Some points of this work probably do not appear in most textbooks.

I do not intend to address academic problems of electronics but fairly simple rules that get neglected or forgotten during schematics and PCB design. Taking those rules serious much wasting of time and money can be avoided.

The line spacing throughout this document is left intentionally large to give the reader space for personal notes.

Actions to do with a CAD or CAE tool are referred to CadSoft EAGLE. In general they apply to other tools (like *Altium Designer, OrCad,* …) too where certain names and operations are named differently.

Special thanks to A. Zaffran at CadSoft Computer GmbH at http://www.cadsoftusa.com for the tables in the appendix. They have been written in German. A translation table from German to English keywords can also be found there.

I appreciate all of critics to improve the quality of this document !

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2 Library

Since the device library provides the smallest entities of a schematic and PCB layout, it deserves most detailed checks and verifications – prior to the actual design of interest. Some general rules:

1. Manufacturers of CAD / CAE systems usually do not guaranty 100% correctness!
2. Please be cautious (even paranoid) when importing third party device models.

2.1 Symbols

Symbol editing requires sound knowledge of schematic design.

Make sure:

1. the symbol of a device is unambiguous and represents the affected part as detailed as necessary.
2. fixed font is used in the symbol exclusively

2.2 Packages

Package design focuses on PCB design and requires skills in terms of:

- reading datasheets of electronic components
- PCB manufacturing
- assembly

Read more in section 6 page 31.

2.2.1 Texts and Fonts

Vector font guaranties constant text size independent of zoom and underlying operating system.

1. **always** use **vector font** in the package drawing
2. Use size 1mm and ratio 13% for name and value placeholders (>NAME, >VALUE)

2.2.2 Outline & Keepout

1. Verify the package outline against manufacturer datasheet.
2. Care for keep out areas (important for SMD as well as THT packages) (layers #39 & #40).
3. Use a line width of 0.13mm for silkscreen, documentation and keepout.
4. Ensure there are no overlaps of silkscreen objects with pads.

2.2.3 Drills & Holes

1. Verify drill sizes of THT-pads (It's very disgusting if the pins of a screw clamp do not fit into the drills.).

2. **Consider maximum drill tolerances guarantied by your PCB house !**

3. Consider alignment pins or bolts connectors are frequently equipped with. Draw holes (preferably in the dimension layer #20 using the command HOLE) where these pins meet the board (Figure 1).

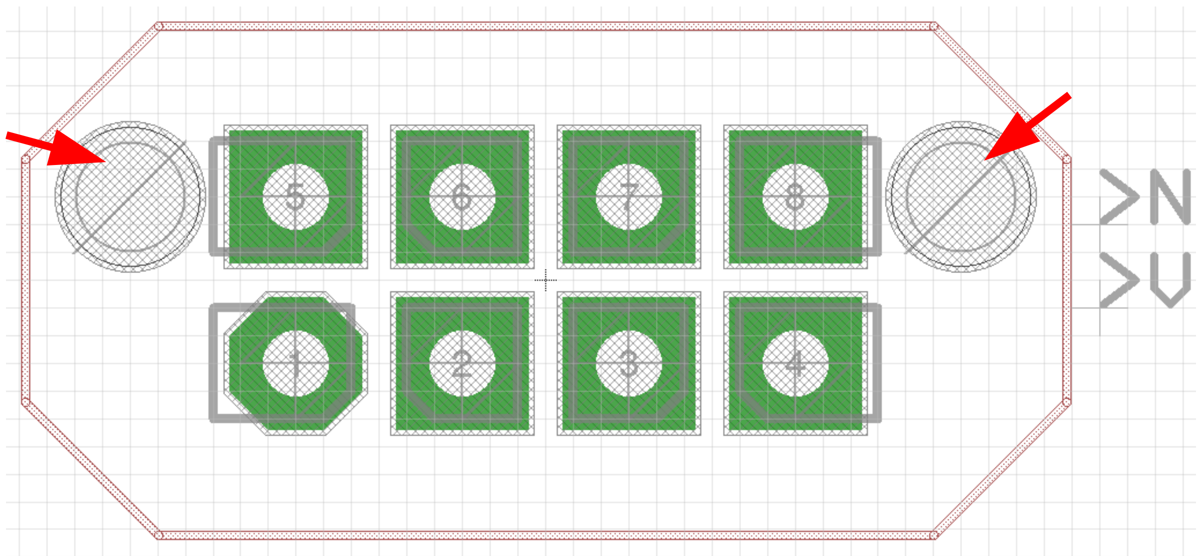

Figure 1: Alignment Pins of a Connector defined in the Library Package Editor

4. Define a proper geometrical center (or origin). Draw the package "around" the origin of the drawing sheet inside the library package editor (Figure 20). The position of the origin affects the placement position of the component on the board. Have a look into the part list exported from the EAGLE **layout** editor (Text 1) ![2]

2 Only if exported from the board/layout the placement coordinates will be put in the partlist.

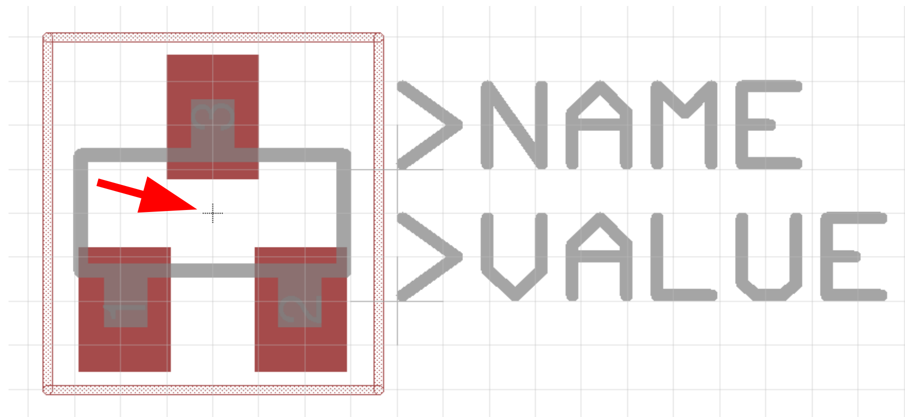

Figure 2: Package Origin

```
Partlist

Exported from example.brd at 2/28/14 10:38 AM

EAGLE Version 6.5.0 Copyright (c) 1988-2013 CadSoft

Assembly variant:

Part      Value      Package     Library      Position (mm)  Orientation

C201      100u/16V   S_6032      rcl          (83.8 80)      R0
C202      2u2/25V    S_0805      rcl          (75.9 81.2)    R0
C203      10n        S_0805      rcl          (69 85.8)      R90
C204      2u2/25V    S_0805      rcl          (71.5 79.4)    R270
FD2401    FIDUCIAL   PASS-ROUND  marks        (89.7 3.5)     R90
FD2402    FIDUCIAL   PASS-ROUND  marks        (11 91)        R90
.
.
.
```

Text 1: Partlist Example with Placement Coordinates

2.3 Devices

1. Ensure unambiguous prefixing of device names in accordance to corporate naming conventions.
2. Make sure there is no mixture of prefixes for the same kind of devices. Examples: All transistors must start with a “T”. All ICs must start with “IC”, all connectors start with an “X”, …
3. Read more in (8).

2.3.1 Pinout

1. Verify the pinout against the datasheet provided by the manufacturer.
2.

3 Schematic

3.1 Device Prefixes

Despite proper settings in the library (see section 2.3 page 8), altering the prefix in the schematic stage is still possible. The rules of section 2.3 page 8 should be enforced here too. Read more in (8).

3.2 Device Numbering

Do the device numbering group wise in relation to their function or the sheet they are placed on ! This eases the later process of PCB design and hardware debugging.

See example below. *CadSoft* provides an ULP that performs this re-numbering page wise in a convenient way: `renumber-sheet.ulp`

Perform device re-numbering before generating CAM files.

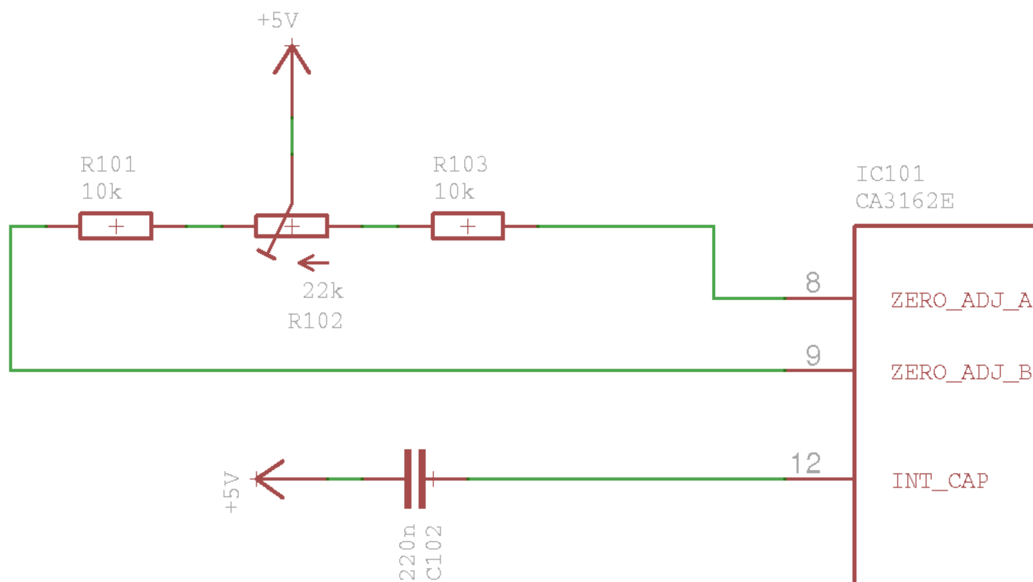

Figure 3: Device Numbering

3.3 Device Values

1. Verify values of ALL devices like resistors, capacitors, crystals, … according to the intended purpose.

2. Give all devices unambiguous values.

   Examples:

   a) A resistor value of 7k5, a capacitor value of 10uF/35V. See section 5 page 30.

   b) The designator „555“ for an IC is not always clear. An LM555 is not necessarily the same as an NE555 (compare manufacturer datasheets).

   c) Special attention deserve components critical for large parts of the board like the voltage regulator shown below. Verify the value is TPS79633DCQ. There is also a TPS79601DCQ which – if fitted erroneously – is going to damage the downstream circuitry seriously.

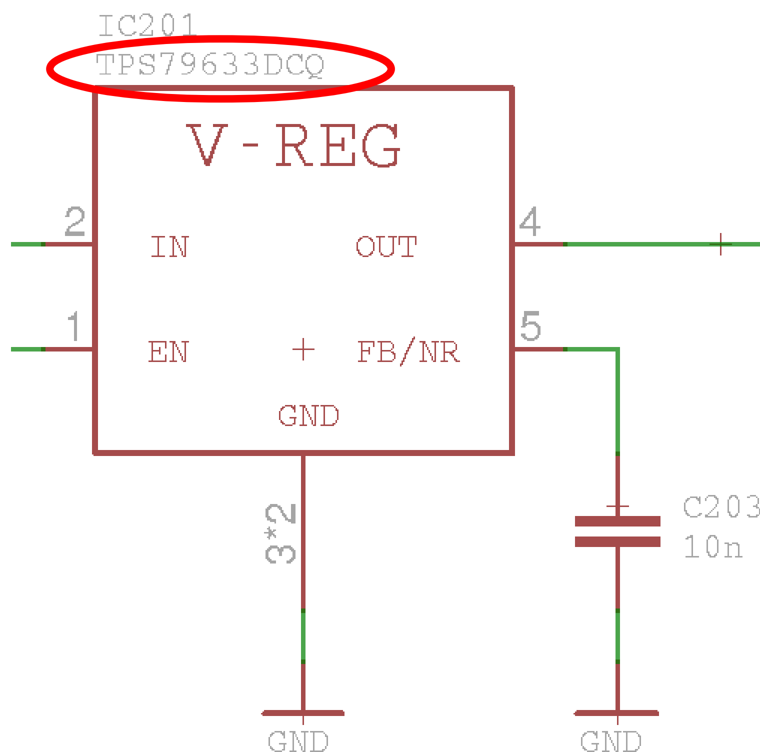

Figure 4: Regulator Value

1. Consider maximum ratings like the **maximum allowed voltage** of capacitors or the **power rating** of resistors. For example a series resistor for a standard 20mA LED operated at 12V may dissipate up to 0,2W heat ! Read more in (9).

2. Ensure there are no white-spaces or special characters (like the "µ") in the value string. They may confuse CAD data importing tools for JTAG/IEEE1149.x or other ATE (automated test equipment). CAD data importing processes frequently understand a white-space as separation character in net – and partlists. ***EAGLE* does not forbid white-spaces in values !**[3]

Potential pitfalls:
By mere copying of devices wrong or ambiguous values may get spread around the schematic.

3 I recommend to *CadSoft* to output an ERC warning in such cases.

3.4 Attributes

Not all parts in the schematic require additional attributes (EAGLE command ATT). Following parts do require an attribute "function":

1. Connectors
    1. Exampe: The power jack X201 in Figure 5 should get an attribute that speaks for its purpose like „Lab. DC Power Jack" .
    2. Do **not** use the value field to display the meaning or function.

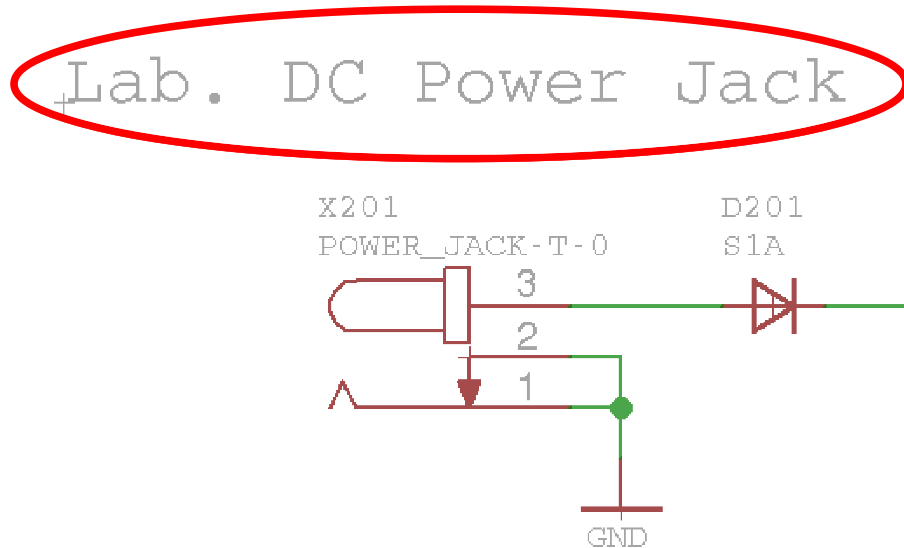

Figure 5: Connector Values

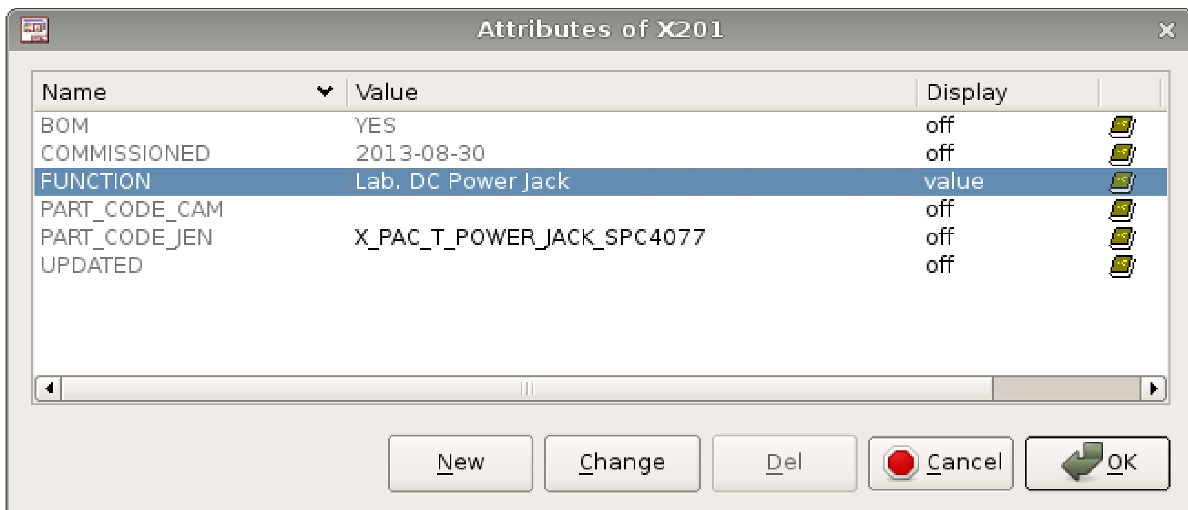

Figure 6: EAGLE Attribute Dialog (command ATT)

2. Jumpers

3. LEDs

Potential pitfalls:

By mere copying of devices wrong or ambiguous attributes may get spread around the schematic.

3.5 Connector/Jumper Pinout Policies

1. Ensure, corporate policies as which pin is to carry GND or any other supply signal have been carried out. Example: Pin #1 of all connectors is tied to GND, whereas the pin with the highest number is to carry +3V3.

2. Verify, that pinout of jumpers prevents dangerous shorts. In the example below an inadvertent dangerous short between any supply rails is impossible.

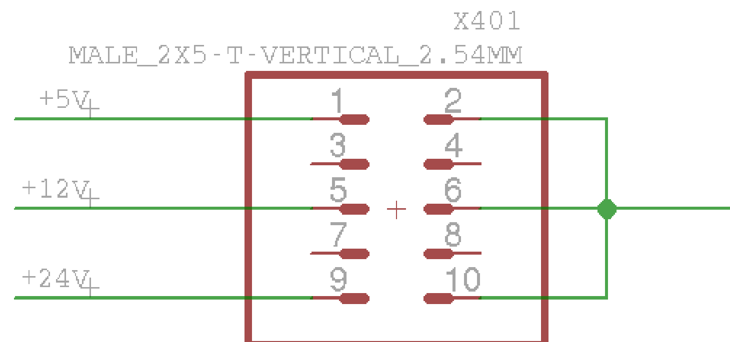

Figure 7: no danger of shorts

3.6 Alternative Fitting

Time is running fast today. The production of a *top, super fast, cheap, high performance, ...* IC made for the mass market may become discontinued after 5 years so that you should have a *plan B* ready without the need to change the PCB layout.

Consider:

1. Component manufacturers notify about the device production status by words like

   full production, not for new designs, obsolete, ...

2. Be also ready for delivery shortages of components.
3. Optionally: Ensure access to unused pins.
4. Ensure access to reserved pins (frequently the manufacturer provides a note like:

   reserved for future use, reserved for test, ...)

In case the alternative component has a footprint differing from the original one: Draw in your schematic the alternative device parallel to the original device and leave a text note for your colleges (see following examples).

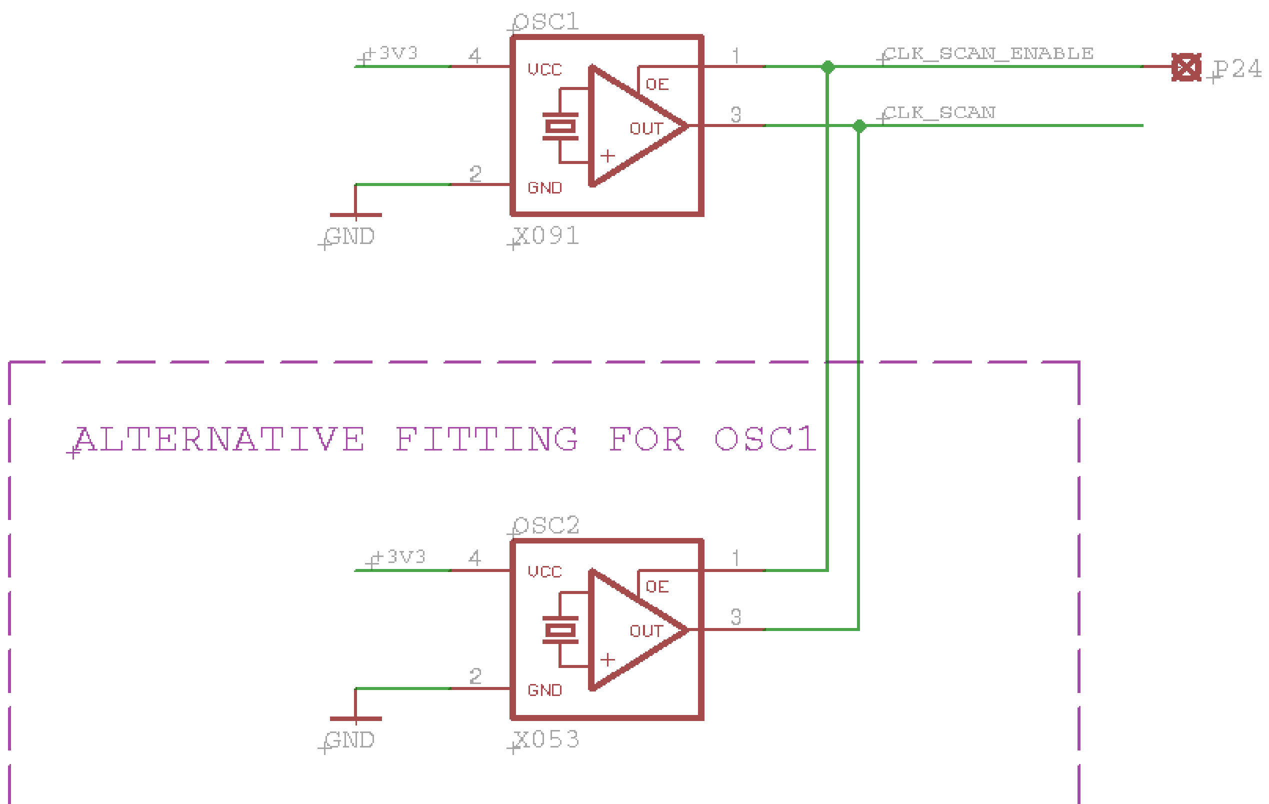

Figure 8: Alternative Fitting in Schematic

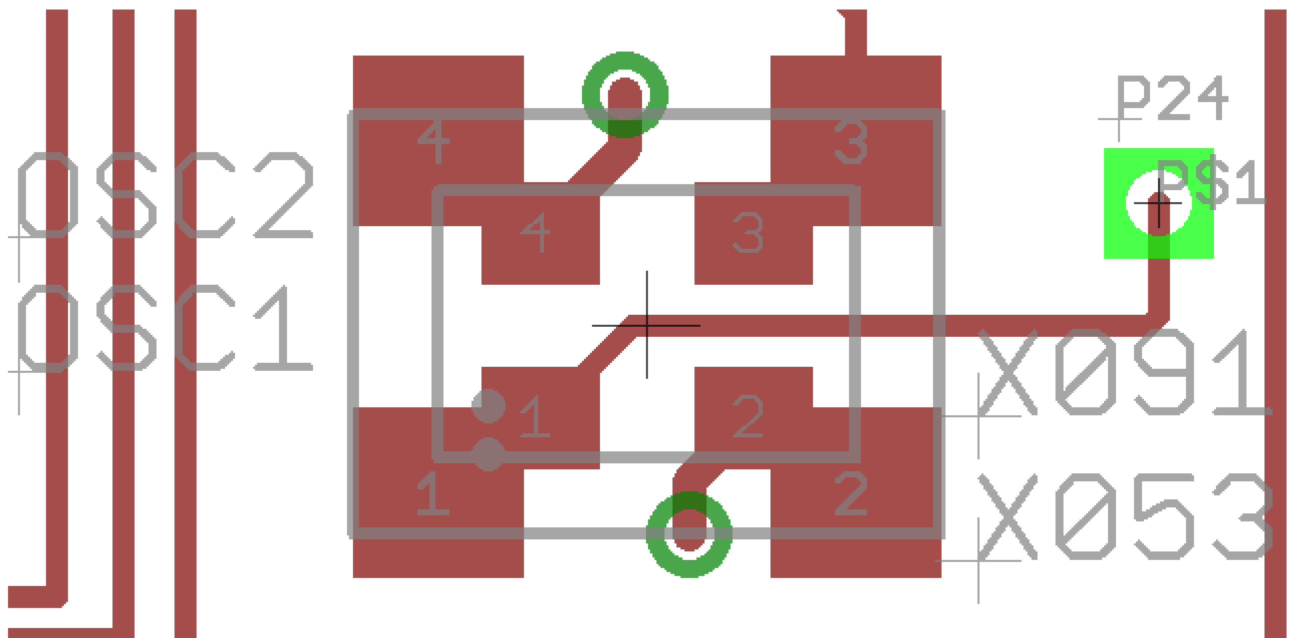

Figure 9: Alternative Fitting in Board Layout

3.7 Minimize Diversity

The smaller the diversity of parts in your design, the better.

1. Use as less different values as possible. For example assembling a board with 20 resistors of 10kOhms each is faster and less error prone than a board having 3 x 8,2k , 7 x 12k, 5x 9,5k and 5x 10k.

2. Combine components in order to achieve the desired value. For example if there are 15 resistors of value 330 Ohms, and if you need another single resistor of 160 Ohms, take two additional 330 Ohms in parallel.

3. This eases ordering and purchasing the components (Prices fall as the ordering amount increases usually.).

3.8 Spare Parts and Accessories

BOM creating tools usually do not care about such items. Ensure availability of:

1. spare parts (fuses)
2. accessories (fuses, cables, screws, washers, nuts, ...)

Examples:

1. A fuse holder with a fuse shipped with provides only this fuse. Make a note in your BOM as where and how many spare fuses are to be purchased in advance.

2. A FPC connector soldered neatly on the board. But, is there a remark in your BOM about the actual flat cable plugged on it ?

3.9 Texts and Fonts

There are various parameters like fonts, text sizes, text ratio, line widths etc. that can be preset so that you are not required to do all these settings all over again when starting a new project. To make things easy just take the file eagle.scr provided in section 9 point (2).

1. Make sure **fixed** font is used in the schematic exclusively.

2. Fixed font guaranties constant text size independent of zoom and operating system when printing on paper.

3. By default fixed font is **disabled** in *EAGLE*[4].

4. Do not use Vector or Proportional fonts !

5. Net labels must have a text size of 0,05 inch or 50 mil.

6. If nets are crossing pages, make use of so called Off-Page-Labels (Figure 19 page 29). These labels indicate the page and coordinates where the respective net re-appears in the schematic.

4 I recommend *CadSoft* to make fixed font default in the schematic editor.

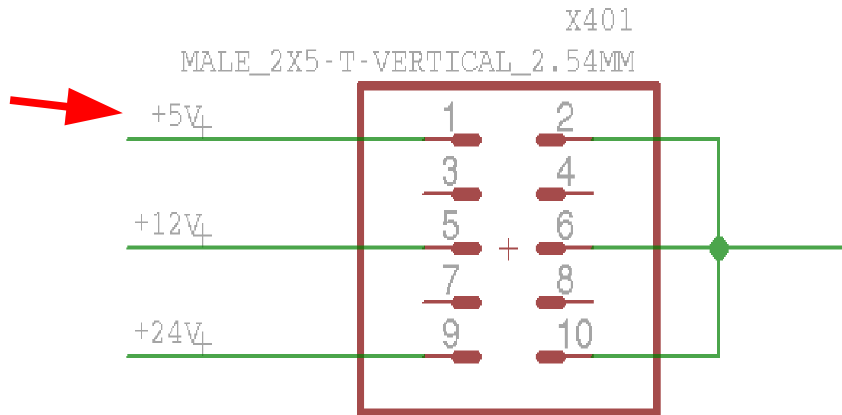

Figure 10: Net Labels

- For texts located in the title block corporate rules apply. See example below.

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Size: A4	Project: PSU	PRODUCT	
Drawn:	Mario Blunk / Blunk electronic	Checked:	Jeremy Miller
Approved:	Dimitry Sacharow		
		Status:	final product
Description:	Power Supply Input (Primary)	Sheet:	1/5
Filename:	psu_v1	Updated:	not saved!

4 5 6 D

Figure 11: Documentation Field

3.10 Version Numbers

Ensure proper version numbers in title block. Read more in (8).

3.11 ERC

Run ERC previously to PCB layouting and generating CAM data.

4 Circuit Behavior

In the schematic phase of a design, a rough forecast of the circuit can be made. Topics addressed in the following are hard – if at all - to simulate.

1. Does your circuitry also work stable and reliable if

    1. optional components are not fitted ?
    2. connectors are open for a period of time ? Open inputs of ICs tend to **float free**, thus increasing power consumption and noise.
    3. Do **not** entirely rely on the ERC (Electrical Rule Check) of your design tool in this case !

2. Optionally: Ensure access to unused pins of components.
3. Ensure access to reserved pins of components (frequently the manufacturer provides a note like: reserved for future use, reserved for test, ...)
4. Does your circuitry behave predicable during reset or power cycling ?

    1. **Note:** During reset the I/O pins of CPLDs, FPGAs, processors and controllers go HIGH-Z or may drive HIGH ! In this phase nets may **float** or cause **dangerous conditions** you have never thought of before like a motor driver bridge shorting VCC and GND.

    2. While in reset state or during power cycling collisions may occur. Outputs may drive against each other. Bus contention on wide bus systems does pose stress to driving devices and leads to increased thermal load on them.

    3. Does your circuitry perform a proper reset after power-up ?

    4. Do capacitors, especially of the reset circuitry, have a path to discharge after power-down ?

    5. Do supply voltages reach their nominal value withing the maximum allowed time ?

    6. Does the power-up sequence of supply voltages matter ?

    7. Make sure the supply voltages die during **power-down** in a sequence that does not cause any damage. **The power-down period may last several seconds !** I recommend a signal – called /PWR_DOWN_ALL – that feds several critical voltage regulators and turns them of simultaneously during that time.

    8. What is the behavior of **not-programmed** ICs like CPLDs, FPGAs after power-up ? For example the I/O pins of the Xilinx Coolrunner II are pulled high by internal resistors of minimal 40kOhm against VCC_IO.

9. What is the behavior of **programmed** ICs like CPLDs, FPGAs after power-up ? In the fitter options of ISE at www.xilinx.com the power-up value of registers may be set.

10. Is a Brown-Out protection required ?

5. Inputs and Outputs of ICs

    1. Is the load at outputs within safe range – even in case of alternative fitted components ? Even if there is no overload, the voltage at outputs changes under load. Digital downstream inputs may not read the state properly in such cases as shown in the example below: The outputs of the operational amplifiers fall to around 1V sinking the LED currents (provided a single supply voltage of the Op-amp). 1V is hard to be interpreted as L signal for downstream devices.

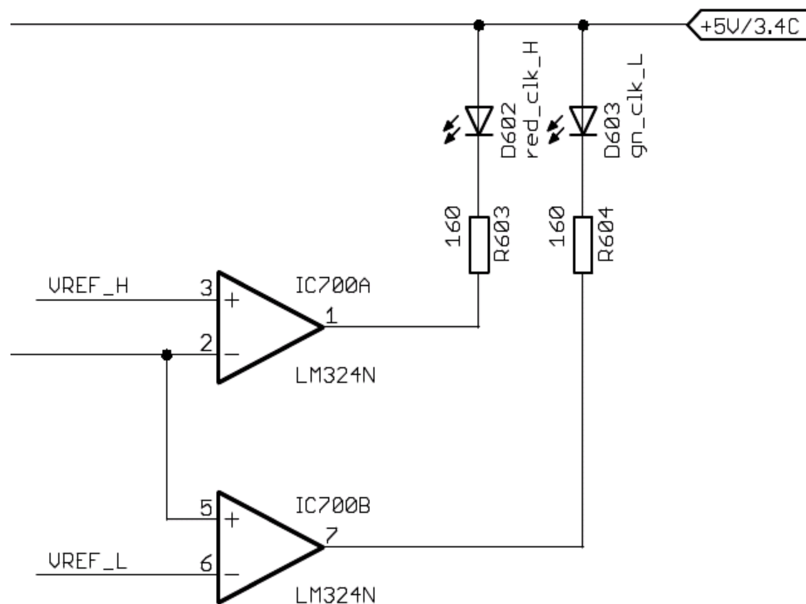


Figure 12: op-amp sinking current

2. Make sure debugging circuitry like LEDs pose as less load to the signal affected as possible. Use MOSFET stages as shown in Figure 13.

3. Do (non-FET) operational amplifiers have DC current paths from their inputs to GND ?

4. Are drivers (like CMOS drivers) capable of driving (multiple) inputs of downstream ICs. Especially mixing of digital device families may lead to “misunderstandings” among them. (See datasheets for output/input voltage ranges, fan out/in) ?

5. Make sure pull-resistors are within manufacturer specified range. If their value (resistance) is too high, the static performance of the line might be okay, but the dynamic switching will be outside the specified range (rise/fall time negatively impaired). If the value is too low, driver pins might be overloaded or line voltages might shift outside safe ranges. Pay attention to specifications of I^{2}C devices.

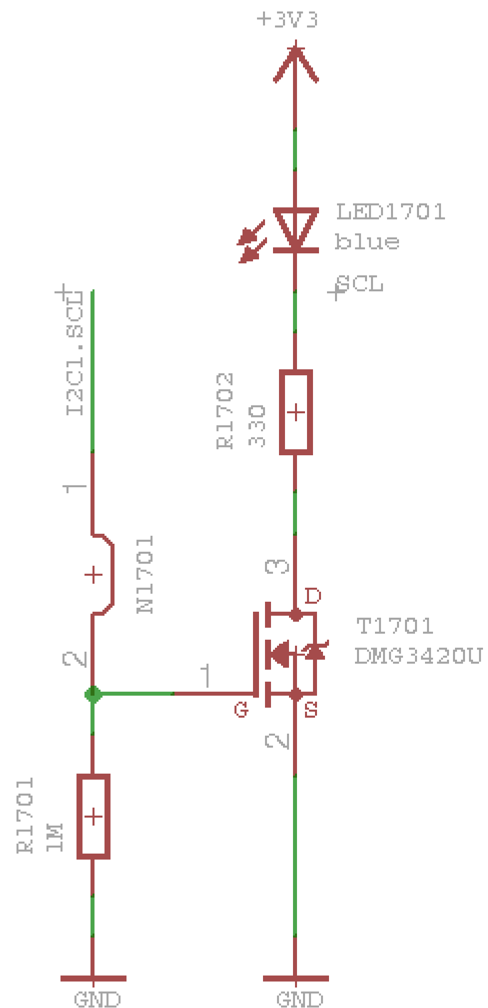


Figure 13: Decoupling Debug Circuitry

6. Operational amplifiers may drive **negative** voltages (when supplied symmetrical) to (digital) downstream devices which may get stressed or damaged in such a case.

7. Avoid **capacitive loads** at op-amp outputs ! Op-amps with feed back loops tend to instability if capacitive loaded. Workaround: Add a series resistor right after the op-amp output to isolate the downstream capacitors as shown below:

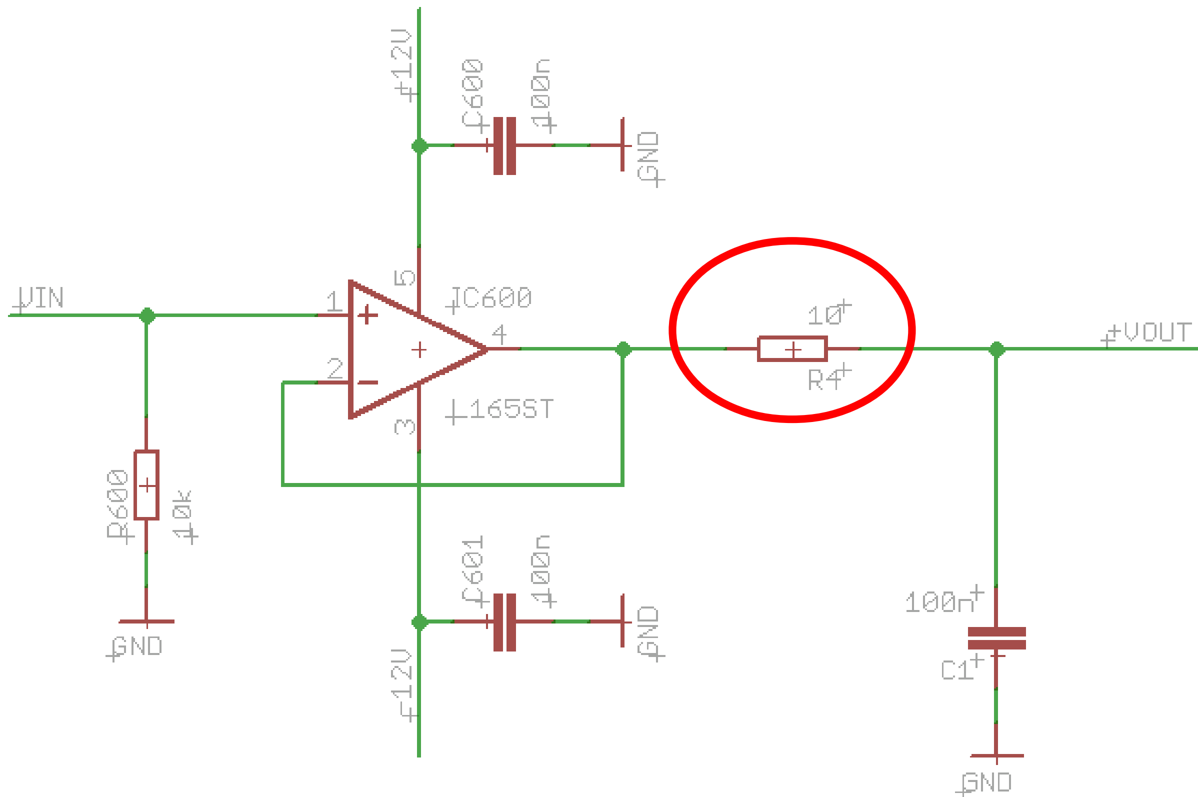


Figure 14: op-amp with isolated capacitive load

8. Are LH or HL edges of digital signals steep enough ? Digital devices show **miraculous** behavior if fed with signals changing too slow. For example if you drive a digital clock input of an XC9572 CPLD by a slow operational amplifier like the well known LM324 you will encounter very strange effects...

9. In harsh industrial environments an output (at a connector) may get shorted inadvertently. Does the driver survive this load at all ? Please take your time to consider this scenario. Replacing the whole unit at customers site may get more expensive than the time you spend thinking on this matter.

10. Probably ESD (electrostatic discharging protection) is an issue for you. *NXP* provides outraging solutions at http://standardproducts.nxp.com/ .

6. I²C issues

- If an I²C slave is to solely receive data (like a DA-Converter) implement a software procedure/function that verifies that the SDA line is **not shorted** to GND. If SDA is shorted to GND for some reason, the I²C master will always see the SDA line low, thus misinterpreting the stuck-at-low SDA as acknowledge bit sent by the slave. The acknowledge bit is the **only means** to verify at a **low level** that the I²C slave is properly connected to the master.

7. Backdriving

    1. If ICs inputs are driven with voltages exceeding the specified maximum ratings given by the manufacturer, backdriving occurs. More or less current flowing into the inputs will accumulate and drain into the power rail, thus raising the voltage there.

    2. Most voltage regulators do **not** sink current into their outputs. So there is danger of **damaging** other devices "living" from the affected power rail.

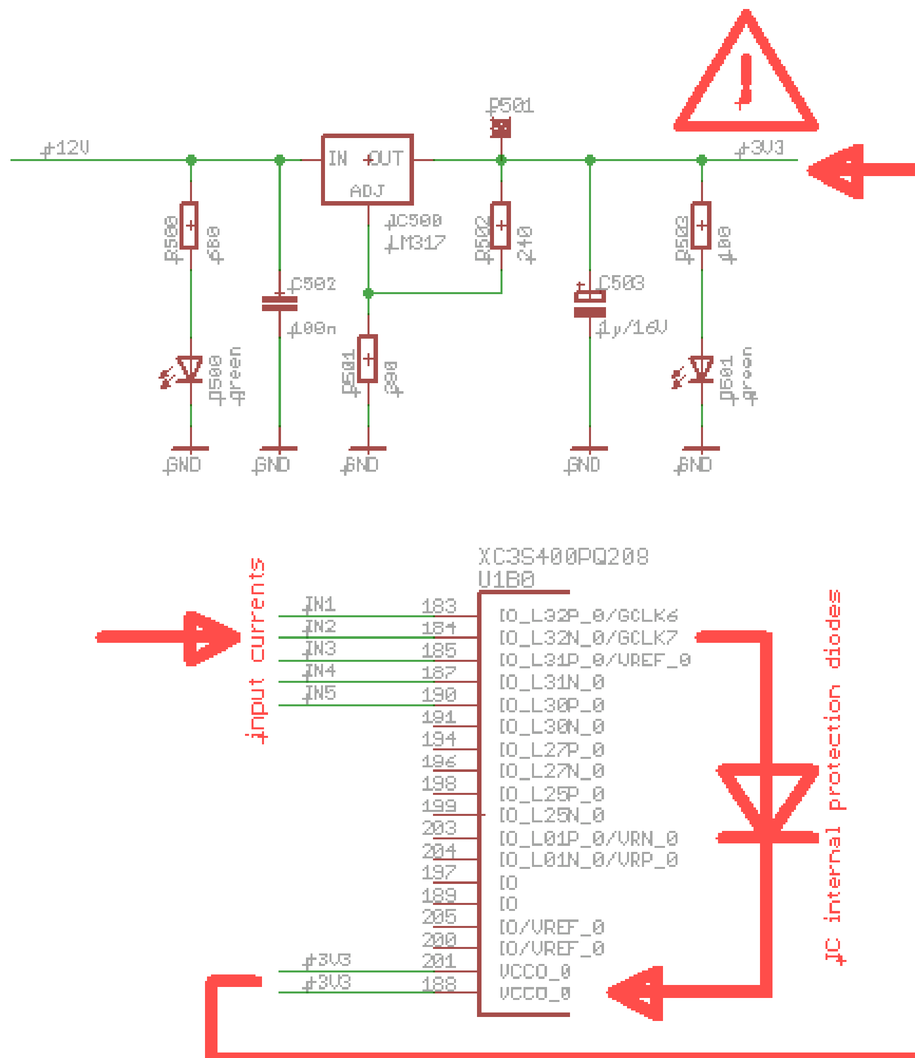


Figure 15: backdriving into power rail

8. Make sure digital ICs are fed with patterns clearly allowed and specified by the manufacturer !

    1. Example: The pattern HLL driven into the inputs A, B and C of an IC causes the device to behave **unpredictable** on its outputs. If you can't avoid such a situation, does it impair the system performance or cause dangerous effects ?

9. Has a minimum of address pins of (FLASH)-EEPROMs been connected ?

    1. Example: When programming or just ID code reading of a W29C020 a succession of 5555h, 2AAAh, ... on the address bus is issued by the processor on at least 15 address lines ! If you tied address pins 15..12 low, because you don't need them in normal mode, the device could not be programmed in-system later on ![5]

10. UARTs, USARTs

    1. Make sure RXD and TXD / CTS and RTS cross each other when traveling between client and host machine !

    2. Verify the pinout of UART pinheaders !

11. JTAG / IEEE 1149.x

    1. Provide termination resistors to GND on TCK and TMS. I recommend from experience to have 300 Ohms each.

    2. Do the boundary scan system (or JTAG-system) drivers have sufficient strength to make a reliable H level on TCK and TMS when loaded with 300 Ohms ? When doing **system level test**, TCK or TMS pins of several boards are to be driven in parallel which reduces the resistive part of the transmission line far below 300 Ohms !

    3. Provide an optional pull-up resistor on TDO of **each** IC on the UUT/ Target-System. ICs not fully compliant to IEEE1149.1 may lack this resistor internally. Not fitting an external TDO pull-up resistor makes less headache than adding one later with airwires and glue...

    4. May the optional L-active **asynchronous** Test-Reset (/TRST) signal become required some time ? Even if your Scan System does not drive the /TRST signal – always have it accessible via a testpad or a jumper ! **Never** tie /TRST hard to VCC or GND !

    5. Layout GND connections generously.

5 This is a very rare case but it indeed happened to me once.

6. Provide means of **switching scan paths** (jumpers, Scan Path Linkers, Scan Bridges, …). For example while system programming the scan chain should be as short as possible (IEEE1149.7 relieves you from that because it allows star topology of scan paths). Another scenario: Optional not fitted ICs within the scan path cause breaks in a serial chain – therefore provide solder bridges between TDI and TDO of the device affected in order to close the break.

7. Alternatively, devices needed for in system programming may be placed in a separate scan path. Short scan paths → less programming duration → lower production **costs** !

8. /WE, /RD or /CE signals should be wired to pinheaders or jumpers to allow driving them by the boundary scan system externally. This way in system programming can be sped up to a large extent. Optionally provide buffers if these signals are to be distributed among multiple UUTs.

9. Programming adapters of programmable logic manufacturers may require a reference voltage provided **by the UUT**, whereas boundary scan systems may **output** a voltage to supply the UUT. Make sure these voltages can't get shorted.

10. Make sure the clock of synchronous RAM ICs can be driven by a boundary scan capable pin in test-mode. Usually in non-test-mode the RAM clock is driven by a PLL or other clock generators. Provide means to "bypass" or disable the PLL in test-mode.

11. Boundary Scan Test systems frequently classify devices during CAD-import **by value**[6]. *Example 1: A single resistor is classified as such by its value 5k1 which is fine so far. If there was a resistor network/array with the same value the CAD-import may output garbage. Make sure no other devices - except single resistors - in your design have the value 5k1 too ! I strongly recommend to give resistor arrays values like 8x5k1 or 8_5k1.*
Example 2: Capacitors of value 100pF may get just a 100 as value for convenience. Imagine the trouble if there are 100 Ohms resistors with just the value 100 ? The scenarios described here occur most frequently but similar cases are also easy to imagine.

12. Pay attention to special pins which determine the IC's test-mode behaviour. Especially some FPGAs have pins like /DONE, PROG or Mode-pins (e.g. M0, M1, M2) which need to be held at a certain level in order to allow full Boundary Scan Test access. Some CPUs require a certain number of clocks applied at TCK while other configuration pins (like a reset input or a mode

6 This way of classifying devices is a result of attempts to speed up test setup time. I'm not if favor of this practice since it brings some risks along.

input) must be high or low for that period of time. I recommend pull-resistors or at least test pads there. In special cases a connection to a connector might be required. Please read the datasheets and BSDL-files carefully !

13. While in test-mode, I/Os may behave different from the full-operational mode. For example, the XILINX Spartan 3 FPGA, pulls all I/Os down via internal resistors. Together with external pull-up resistors, the result is a voltage divider. Thus, the voltage at the pin may be outside of specifications, which results in unpredictable test results.

14. There might be a pre – and a post configuration BSDL file required for some ICs ! The post-configuration BSDL should be output by the logic synthesis tool.

15. Does power sequencing matter ? (see point 4 page 18)

16. Provide means for a full galvanic separation of the scan path signals (incl. GND) from the scan master.

17. Avoid driving the scan path signals into the UUT when powered down.

18. Provide means to monitor and limit the power consumption of the UUT.

19. See reference (7) for more.

12. Design for Test (DFT)

    1. **Note:** Your product will make it to series production some time.

    2. Care for safe, fast and easy testing of the board in advance !

    3. Contact PCB and assembly houses during board design.

    4. Provide GND and power supply test points to connect instrumentation to.

    5. If the majority of devices is of analog nature the board is likely to be tested by ICT (In-Circuit-Test) or manually. Have you provided test pads on critical signals ?

    6. Multilayer boards fitted with BGA packages usually don't allow **mechanical access** to signals !

    7. Digital areas of the board should be tested by Boundary Scan/JTAG according to IEEE1149.1/6/7. See point 11 page 24 .

13. Make unused IC pins accessible.

    1. Do not just hard wire them to GND or leave them open as this makes extensions or modifications difficult or impossible. Connect them to a well accessible solder pad nearby.

    2. This also applies for pins that are named with NC or “no connect”. NC means: *The pin is not bonded or wired inside the IC.* In case there will be a **replacement** by a similar device later, this pin may become important. See following example: A successor of the W29C020, an AM29F040 has pin 1 serving as address input A18. If left open in the original design (where it was an NC pin), the successor IC would have A18 floating free – **fatal !**[7]

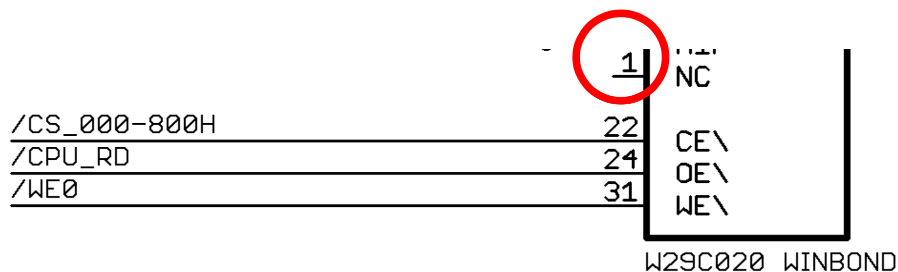


Figure 16: NC pins may become a problem

    3. The next example shows two left over operational amplifiers of a quad Op-amp (LM324). Should there be a modification later they are accessible since they are “soft” wired via R129.

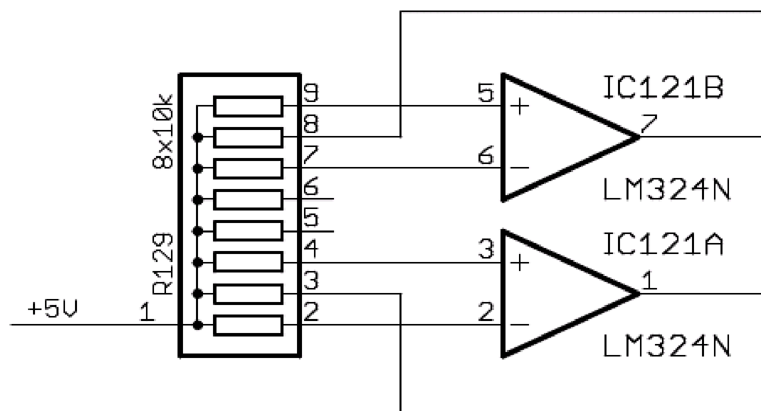


Figure 17: soft tied leftover op-amps or gates

7 Some datasheets do not allow to connect NC pins at all, which makes in-advance-connecting of NC pins impossible.

4. If you also wire these pins with solder pads or pin header mechanical access becomes simple. Apply this method when using fine pitch packages like TQFP-144 or BGAs.

5. I also recommend to wire these pins with pull resistors externally.

6. The example below (left hand) shows 7 unused pins of a Xilinx Cool-Runner which have been wired to solder pads (right hand).

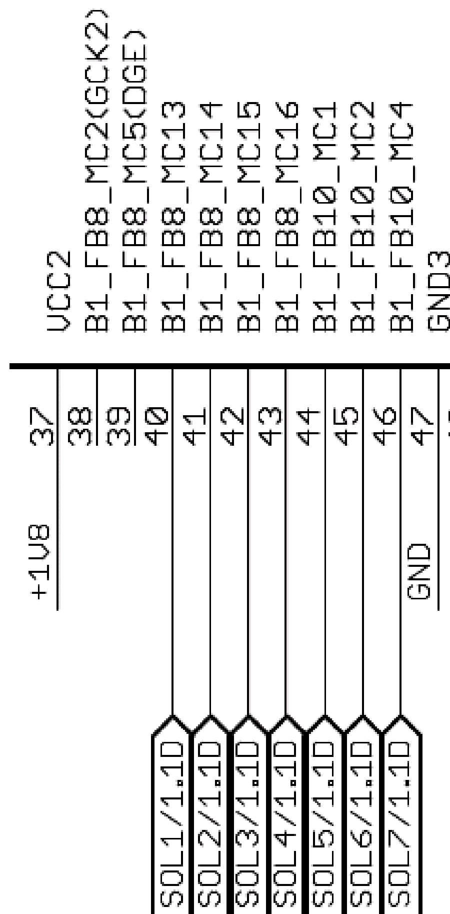


Figure 18: Solder Pads

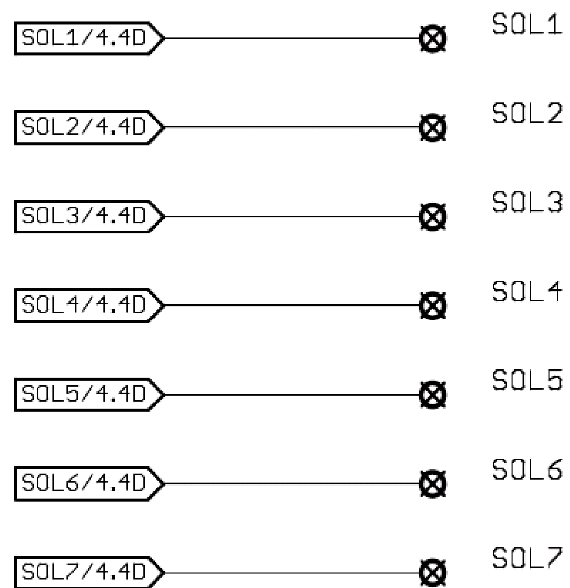


Figure 19: Solder Pads

14. Have you named **all** nets explicitly ? Even those without **label** ?

    1. Just relying on automatic naming of your design tool does not give much of value as far as later board debugging goes. E.g. a net name „CATHODE_RESET_LED“ does say more to your college than just „N$1701“.

    2. Give hierarchic net names like: MCU_OSC_IN, MCU_OSC_OUT, MCU_JTAG_TCK, MCU_JTAG_TMS. This eases routing the signals later in the board layout. If you consider using the autorouter or merging schematics this measure is a good preparation.

15. Have you defined **net classes** ?
    1. For later layout design its important to define track widths and clearances of certain nets **in advance**.
    2. Contact your PCB house as far as minimal structure dimensions goes.
    3. Read more on net classes in (8).

5 Circuit Reliability

This section addresses selection of electronic components regarding their maximum ratings. Rules of thumb are given to obtain a reliable product.

Ensure device accuracy, drift, noise, operating temperature range meet given constraints.

5.1 Transistors

maximum rated voltage (V_{ce}, V_{be}, V_{ds}, V_{gs})
$V_{xx} > V_{nom} / 0.8$

5.2 Capacitors

maximum rated voltage of capacitors (V_{max})
$V_{max} > V_{nom} \cdot 2$

5.3 Resistors

maximum rated power of resistors (P_{max}) at maximum environment temperature
$P_{max} > P_{nom} / 0.75$

For further reading see (5).

6 PCB Layout

In contrast to schematic design, the PCB design requires profound knowledge of:

- material properties
- CAM files (Gerber & Drill Data)
- fabrication processes

Depending on signals (edges, frequencies) traveling on the board these problems deserve special treatment:

- EMC issues
- SI issues

6.1 Prior to Routing

Before routing tracks numerous precautions are to take. Refinement is still possible in later stages of the design.

6.1.1 Board Outline/Dimensions

1. Make sure board dimensions are well defined in layer MEASURES (see Figure 31 page 43).
2. Ensure a text size of 2mm for measures.

6.1.2 Mounting Holes

1. Make sure the hole diameter (including tolerances) is correct.
2. Optionally: Provide electrical connection to protective ground.
3. Optionally: Use the "lock" command to nail down holes so that they can't be moved inadvertently.

6.1.3 Placement in General

Usually a coarse placement takes place at this stage. Refinement is conducted later while routing.

1. Make sure devices on top or bottom side do **not overlap** !

2. Consider heat sinks and other accessories that usually require more space than you think (Figure 20).

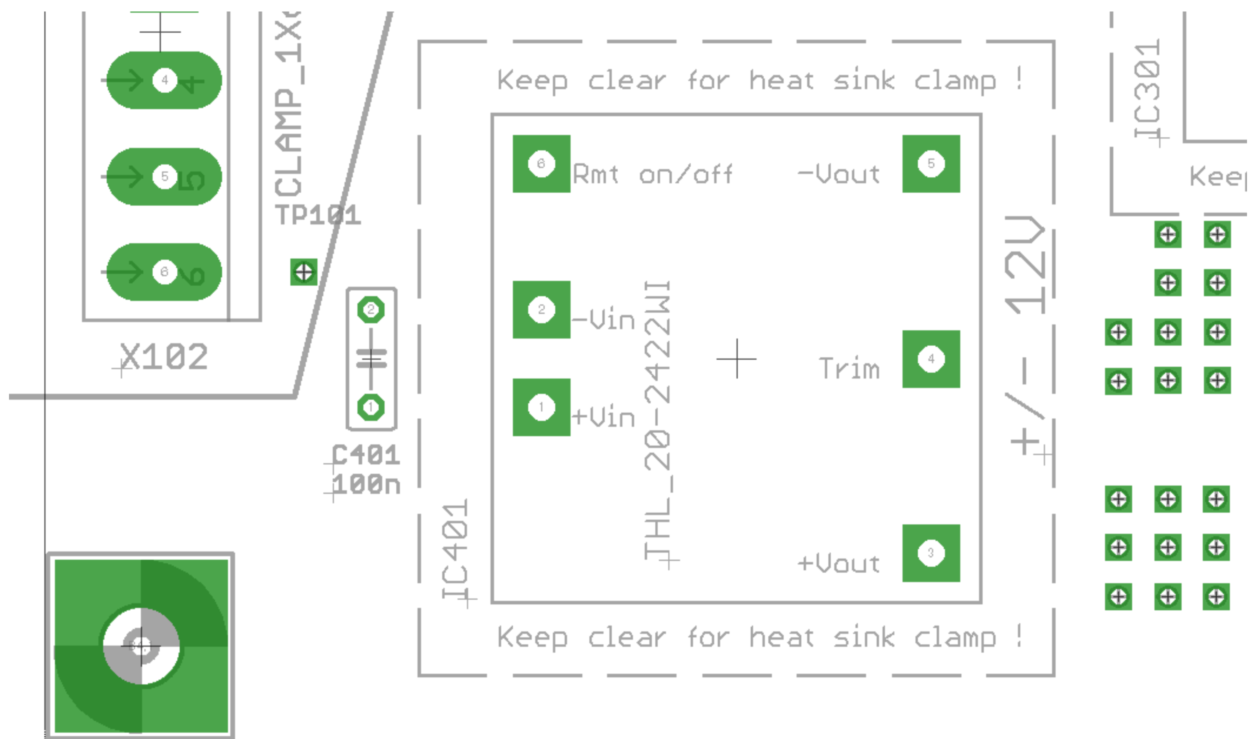


Figure 20: Clearance for Heatsink of a DC/DC Converter

3. In case you plan to **manually** assemble the board (even when using SMD): As a courtesy to your colleges consider following (as far as signal integrity allows of course):

    1. Resistors of equal value may be placed in groups.

    2. Diodes and capacitors may be placed with their cathodes/poles pointing to the same direction.

    These measures make the assembling less error prone, faster and **cheaper**.

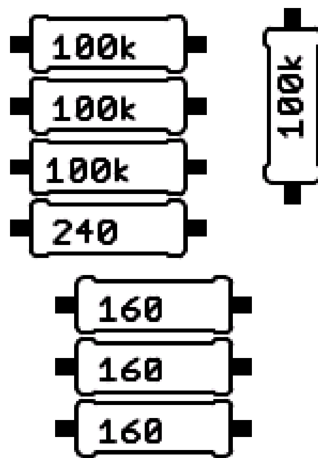


Figure 21: Resisor Grouping

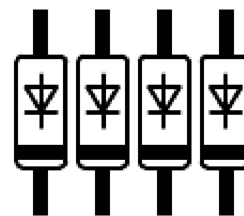


Figure 22: Diodes Orientation

6.1.4 Placement of Connectors, Jumpers, Switches, LEDs, Displays

1. Make sure, those components have been placed to meet the requirements and constraints of the target application.

2. Take constraints of mechanical engineering department into account.

3. **Your customer determines, not you alone !**

4. Have you marked pin 1 of connectors ? If possible the pin 1 mark should be in the silk screen. The folks setting up the assembly line will appreciate it.

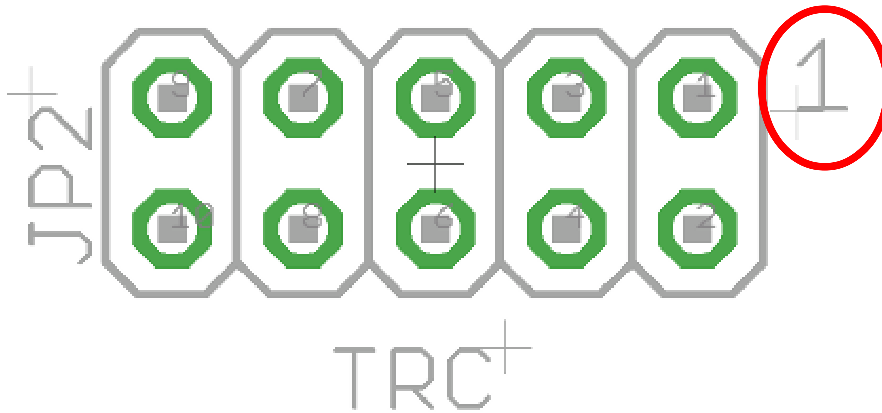


Figure 23: Pin 1 Mark

5. Optionally: Use the "lock" command to nail down these devices so that they can't be moved inadvertently while place & route.

6. Optionally: Arrays of diodes or LEDs should have all the anodes pointing into the same direction (See Figure 22 page 33).

7. Ensure sufficient clearance around headers and connectors so that the counterpart plugged there does not collide with other neighboring devices[8]. This measurement can be supported and prepared in the library. See section 2.2.2 page 6.

8. If your target application poses mechanical stress on connectors, I recommend **not** to place them directly on the board as pads tend to get loose or ripped out. Place those connectors in the **housing walls** instead.

8 Most THT packages shipped with the EAGLE library do not have a keepout frame. I strongly advice for a keepout frame around THT packages.

6.1.5 Texts and Fonts

1. **always** use **vector font** in the PCB drawing. Vector font is also required for production of your PCB as varying text size may result in **shorts** when using proportional font in copper/signal layers[9]. By default vector font is **disabled** in *EAGLE*[10].

2. Ensure proper version tag either in silkscreen or top or bottom side copper like “RS232-IF_V3.2b”.

3. Place a text in the copper like “TOP” or “BOT” to identify faces.

4. Make sure ALL parts have been smashed (EAGLE command “smash”)

6.1.6 Reference marks / Fiducials

1. Contact EMS house as how and where reference marks should be placed on the board. At least two fiducials are required by assembly machinery !

2. Make sure at least 2 reference marks are listed in the partlist exported from inside the board layout editor (see Text 1 page 7).

9 If Gerber Files are generated with the CAM Processor all texts will be rendered to vector font in the Gerber Files.

10 I recommend *CadSoft* to make vector font default in the board layout editor.

6.1.7 Solder Pads for Modifications or Extensions

When in prototype phase, you are required to make changes on your board like additional pull resistors or just a status LED.

1. As precaution provide solder pads **in advance** as shown in the drawing below framed **red**. Solder pad arrays of this kind can be made by pads or lots of vias. Pads, as shown in Figure 24 are “real” electrical devices (with symbol in schematic and package in layout). Vias in turn can be placed in the board only. They do **not** have a counterpart in the schematic. Modifications or extensions soldered there look relatively good and are of stable mechanical nature.

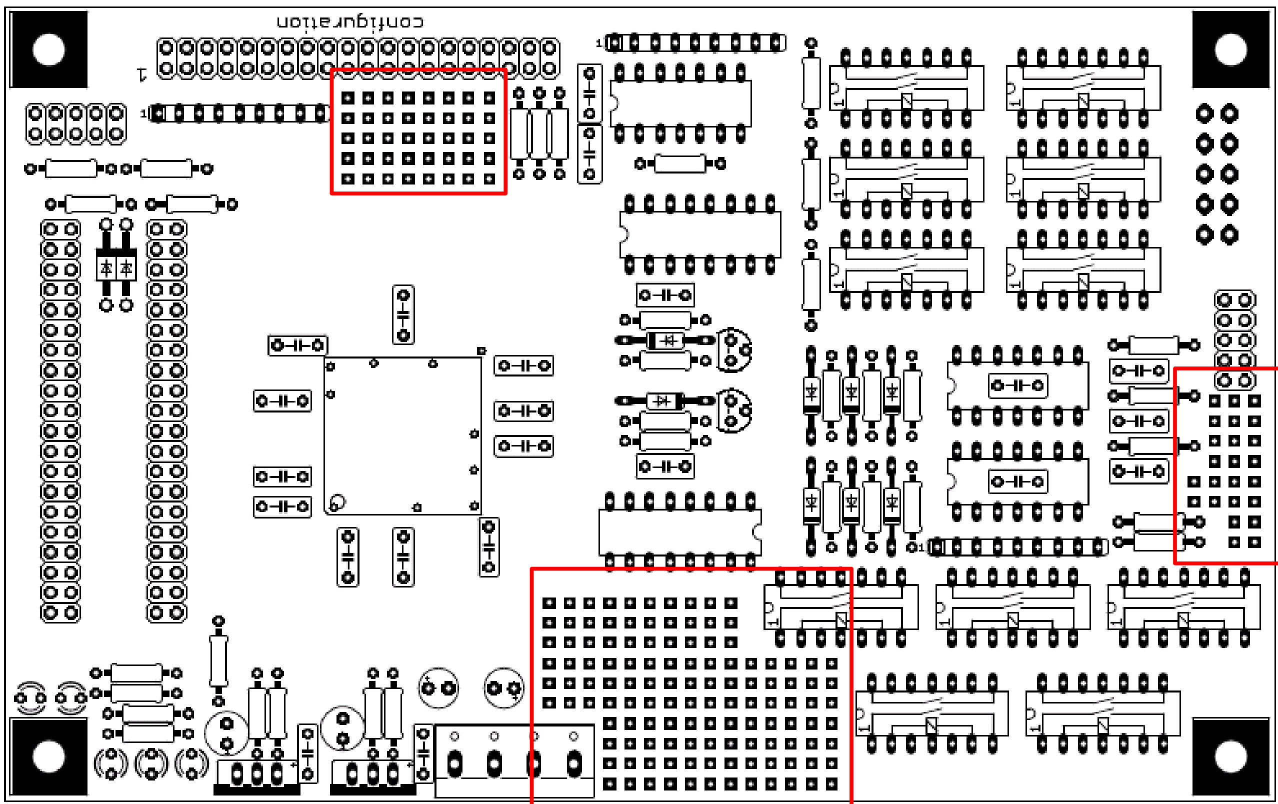


Figure 24: Solder Pad Arrays

Note : If vias should be “solderable”, check the “via thermal” option in the DRC settings. This way vias become “solderable” . Otherwise they get embedded into the surrounding copper plane without thermals, which draws away all the heat that comes from the solder machine (see below).

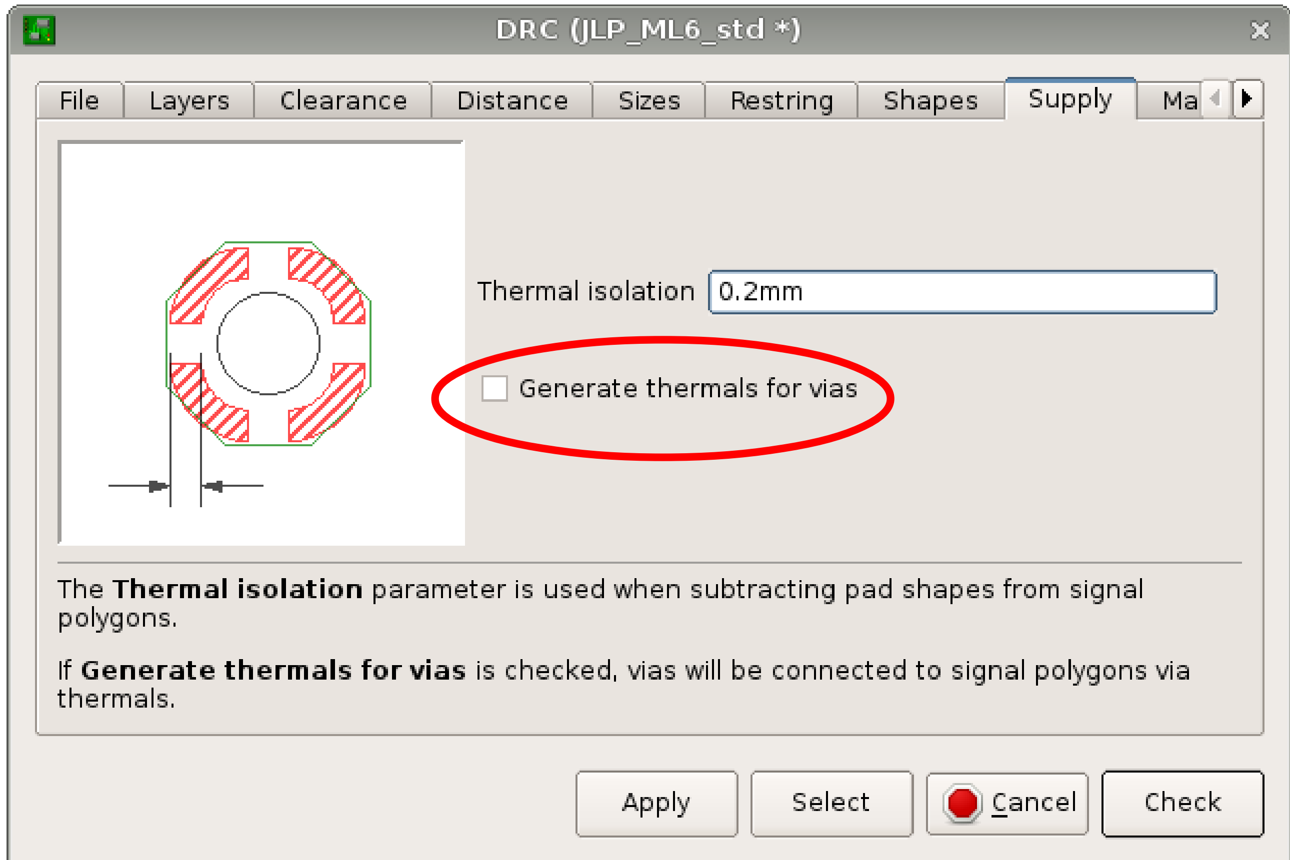


Figure 25: Via Thermal ON/OFF Setting in DRC

6.2 While Routing

1. Run DRC from time to time and **finally** before generating CAM files !
2. Consider the maximum current load of copper tracks (see Appendix). Unavoidable **critical** conditions should not lead to **blown tracks**. See also section 4, page 18, point 4 In a harsh industrial environment an output may get shorted inadvertently temporarily.
3. Optionally: Avoid vias inside a pad as the solder may drain into the via hole. The solder left on the actual pad may become to less for a reliable pin-pad joint. **Contact EMS house !**
4. In the proximity of screw clamps or connectors the board is probably going to be stressed heavily. Avoid tracks in top layers where wires are inserted. In Figure 26 red arrows indicate the direction wires are inserted from. They may **disrupt** a track or scratch the solder stop lacquer – **danger of shorts !**

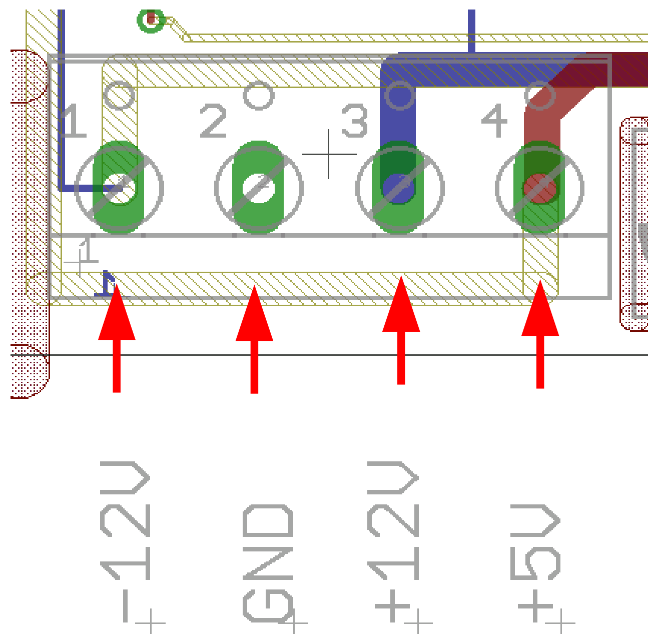


Figure 26: Avoid Tracks near Screw Clamp

5. Generously, as far as possible, provide copper areas on pads or mounting holes in order to improve mechanical stability. Usually device models provide just a minimum of copper around their pads.

6.2.1 Solder stop lacquer / mask

Make sure vias are **covered** with lacquer/coating always.

Note: If the board is to be **wave soldered** shorts between vias and pads may result otherwise ! Keep vias free from solder stop lacquer/coating in **exceptional** cases only. Figure 27 gives an example of how to set this rule in the DRC menu: All drills with a size greater than 0.6mm do **not** become covered with lacquer[11] and thus will be exposed for soldering. This setting applies for all vias.

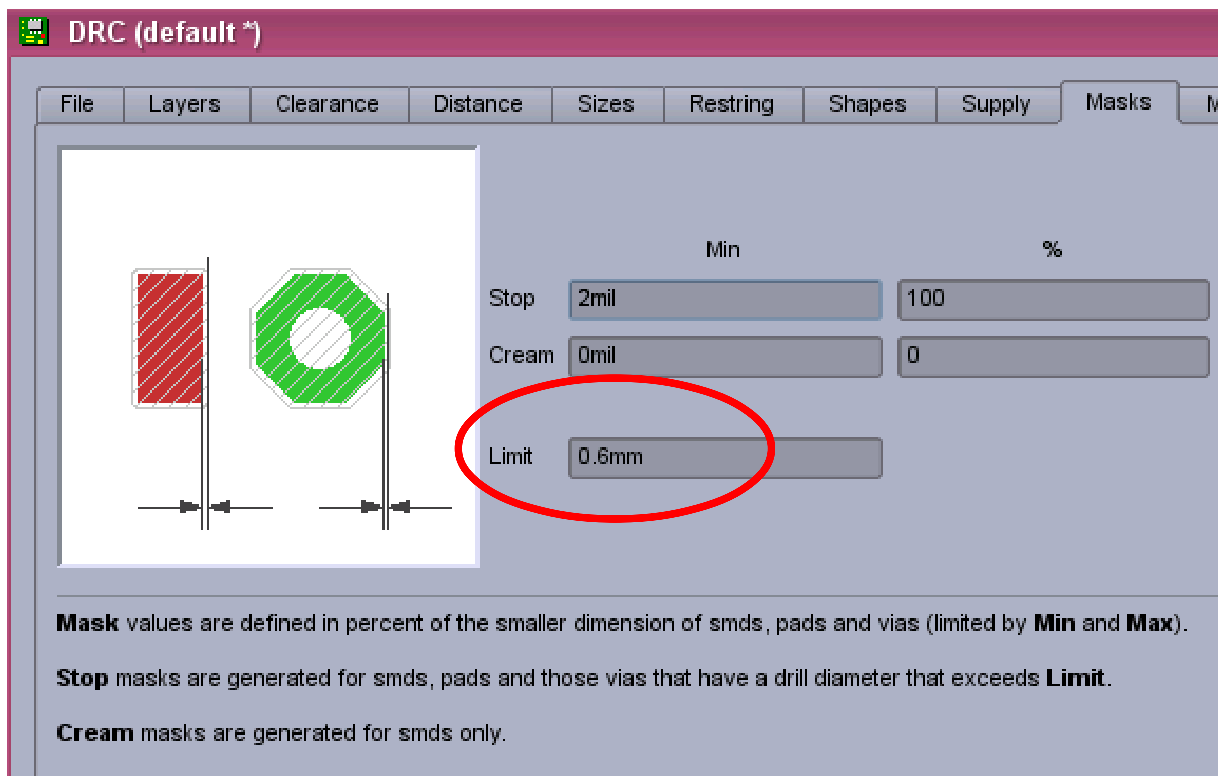


Figure 27: Solder Stop Mask on Vias in DRC

11 The default setting here is 0 mm. Means no vias are to be coated with lacquer. All vias will be exposed for soldering.

6.2.2 Polygons

Polygons are a great invention. By drawing a polygon in a copper layer and naming it with a signal name, like GND, lot of routing time can be saved. Polygons improve EMC and SI behavior. The **disadvantage** is: Polygons may **fall apart** during manual or automatic routing.

1. To make sure polygons are still integer run the command "ratsnest" from time to time. The ratsnetst result is shown in Figure 28.[12]

2. Run “ratsnest” previously to generating CAM files.

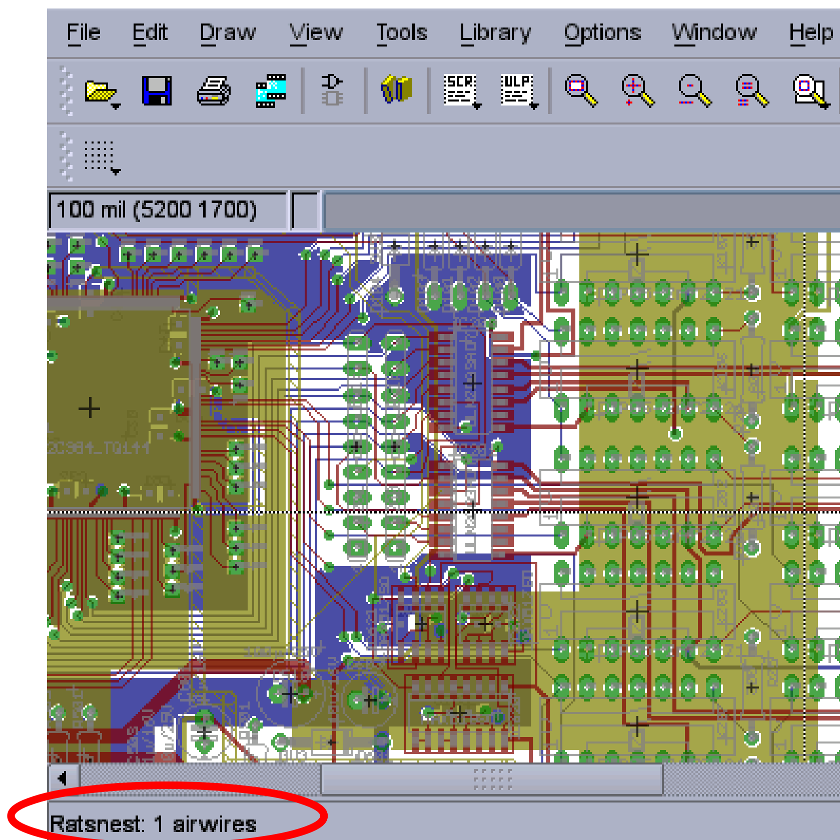


Figure 28: Ratsnest Output

3. Verify, layer #19 (unrouted) does not contain any objects after running “ratsnet”.
4. Another critical issue are bottlenecks from one copper area to another. Figure 29 shows an example. Red marked is a very narrow pass-through of copper connecting the left and the right area. This very narrow "bridge" spoils signal integrity and may be blown when carrying high currents. Ensure integrity of polgons.

12 I recommend *CadSoft* to make those airwires flashing so that they can be found easily. Especially very short airwires are hard to find in large drawings.

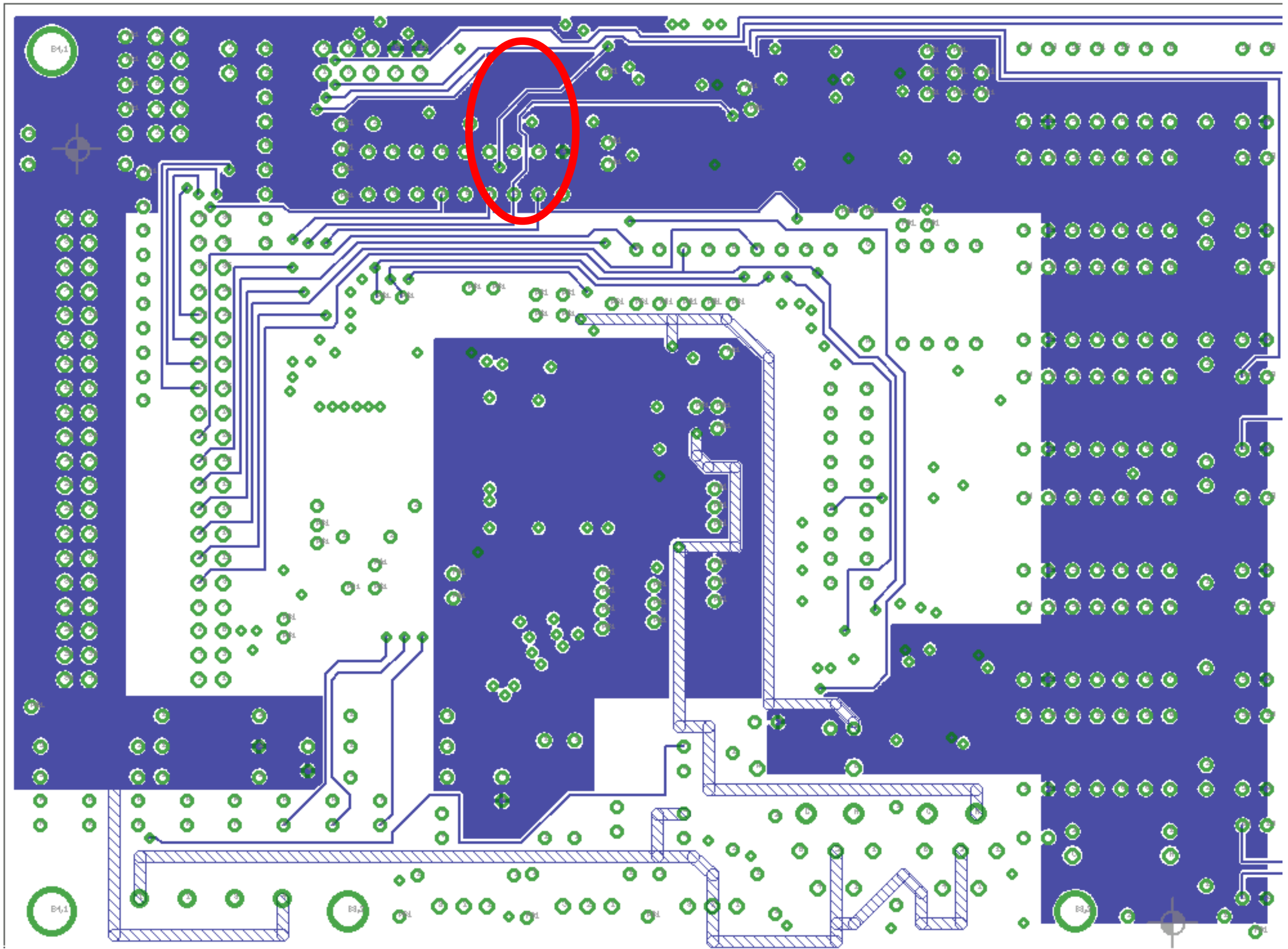


Figure 29: Bottleneck in a Polygon

6.2.3 Slitted Holes in Inner Layers

By default the shape of a long or offset pad is not copied into inner layers. Here an example:

Figure 10 shows these pads as they appear in the top copper layer which is fine so far. In layer millings (number 46) the contours of the plated millings are drawn in turquoise color.

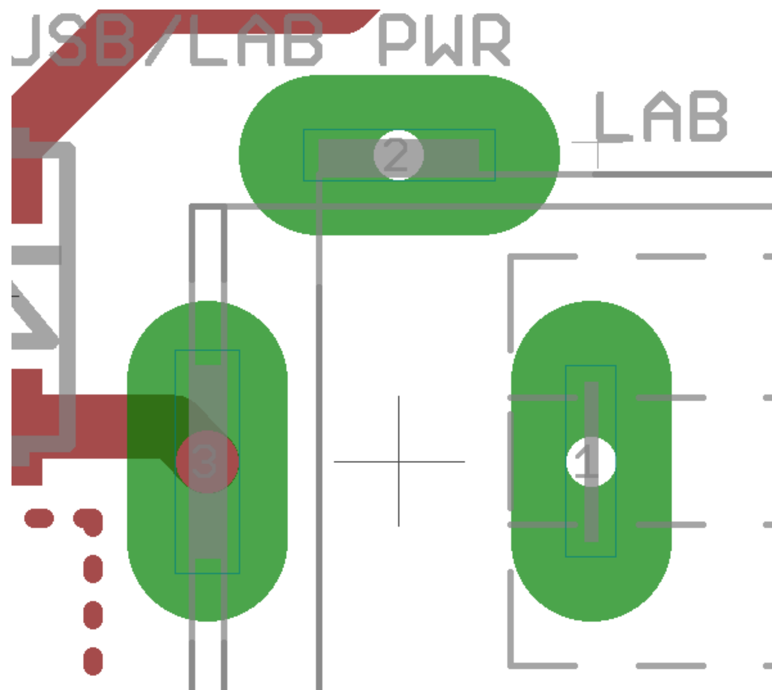


Figure 30: Slitted Hole in Top Layer with Millings

Figure 30 shows the inner layer #15 (which is the GND polygon) and the pad shapes in that inner layer. And here comes the bomb:

The rectangular plated milling around pad 3 (framed red) causes a dangerous short between the actual pad and the surrounding plane !

WARNING !

The EAGLE DRC tool does not detect shorts caused by objects drawn in layer millings !

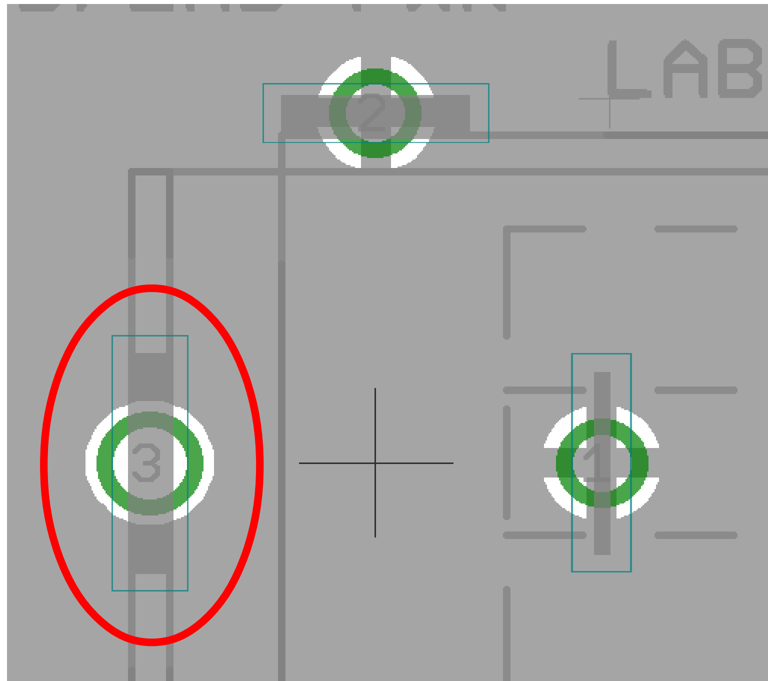


Figure 31: Slitted Hole in Inner Layer with Millings

Figure 32 shows a partial solution using the EAGLE ulp

`make-long-pad-inner-layer.ulp`

with the drawback of missing thermals around pads 1 and 2.

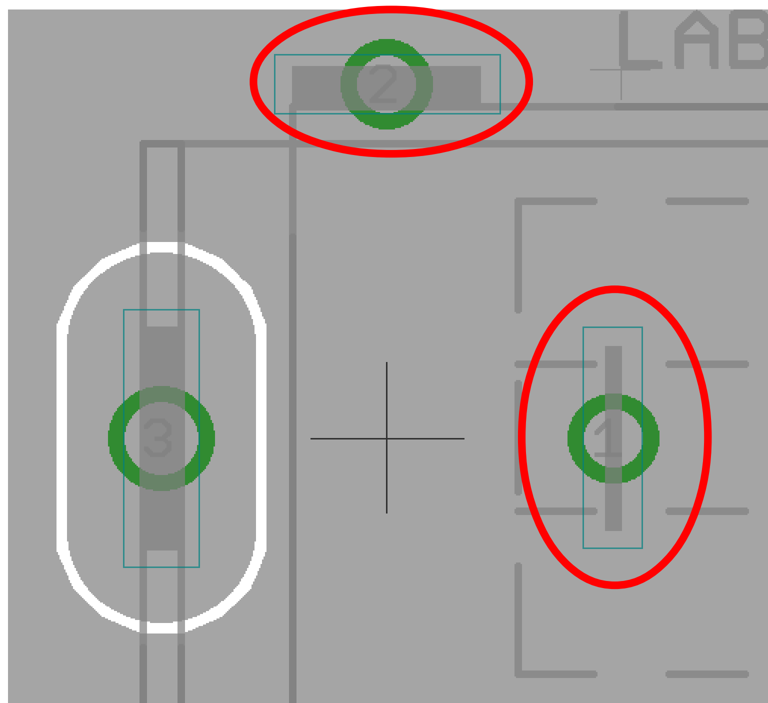


Figure 32: Inner Pad Shape after make-long-pad-inner-layer.ulp

A safe but more laborious solution is shown in Figure 33. Thermals and restring have been drawn using the command WIRE. Cut-Out polygons have been placed. The outcome in the Gerber files is shown in Figure 34.

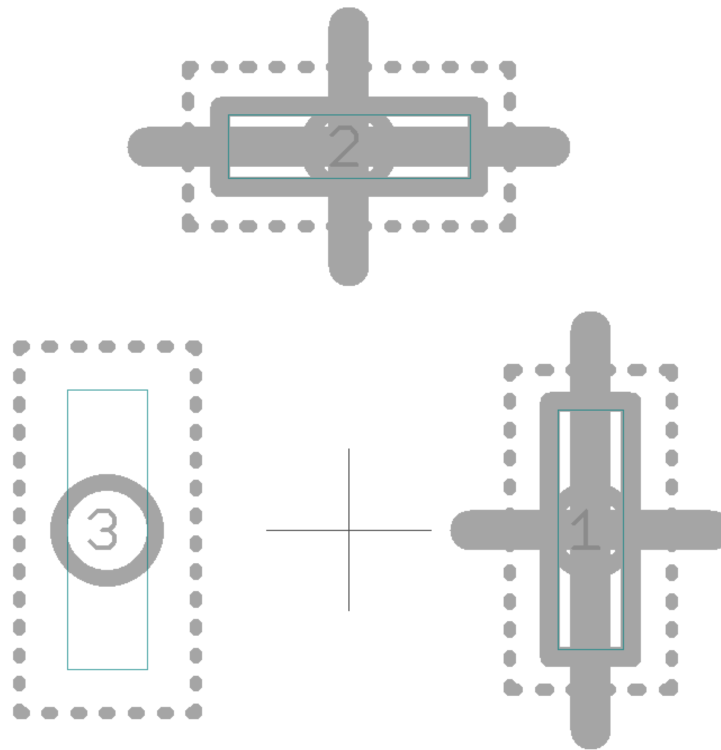


Figure 33: manually drawn thermals and cut-out polgyons

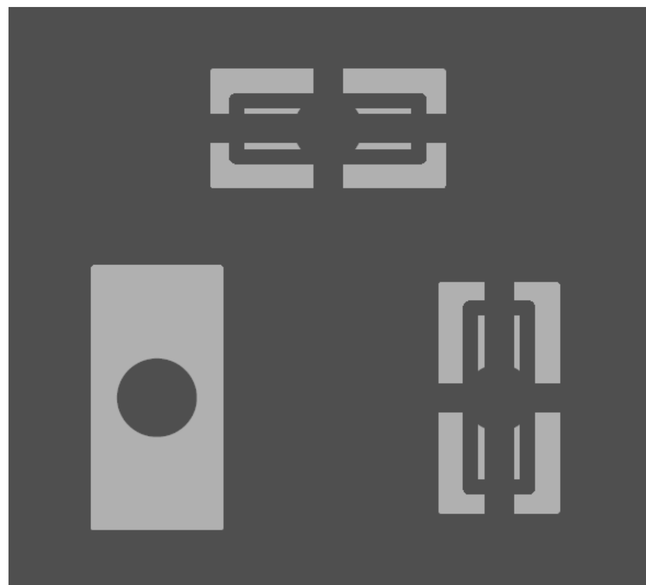


Figure 34: Result in Gerber Data

So the subject of check is:

Make sure there are no shorts caused by plated millings in inner layers !

6.2.4 Silk Screen Issues

The silk screen is an **option** for PCBs but not a must. In general the PCB maker charges you with an extra price for silk screen. It is useful for fitting parts on the PCB and for service and maintenance as well. Unless it is pointed out, no silk screen will be applied.

WARNING :

NOTIFY PCB MANUFACTURER IF YOU NEED SILK SCREEN ! MAKE WRITTEN NOTES IN CAM FILES ABOUT IF AND WHERE SILK SCREEN IS REQUIRED !

6.2.4.1 Overlaps with Pads

Ensure, silkscreen objects do not overlap with pads !

To verify objects drawn in the silk screen layers - usually tPlace/bPlace (21/22) and tNames/bNames (25/26) – do not overlap with pads:

1. display only layer tPlace (21), tNames(25) and tStop (29)
2. run DRC
3. display only layer bPlace (22), bNames(26) and bStop (30)
4. run DRC

See example in Figure 35 page 46.

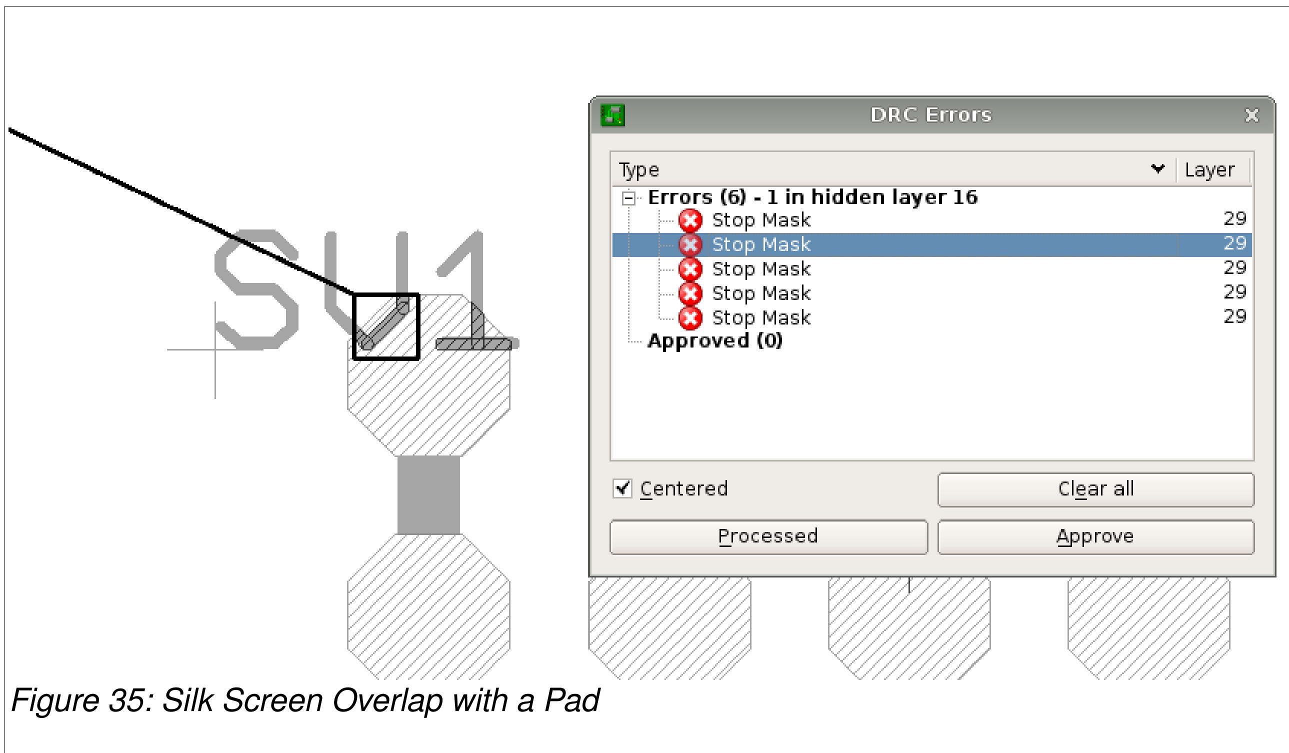


Figure 35: Silk Screen Overlap with a Pad

Usually the PCB house cares for such issues by clearing the pad from silk screen data with a Gerber Editor (see page 60 point (8)). But as a good engineering practice you should care for these overlaps at the design stage.

6.2.4.2 Overlaps with Texts in Top/Bottom Layer

Make sure silkscreen does not overlap any texts placed in top or bottom layer.

6.2.4.3 Attribute FUNCTION

Connectors, Jumpers, LEDs, switches frequently bear the attribute FUNCTION. If the function is to be part of silk screen, make sure text size, ratio and layer meet the PCB manufacturer specification (see 6.2.4.4 page 47).

Make sure the function attribute is visible and transposed in layer tPlace or bPlace in order to get printed on the board.

6.2.4.4 Text Line Width (Ratio)

Please ask the PCB maker for the **minimal line width** they can guaranty. For standard PCBs 0.15mm applies in most cases.

The ratio (in %) of line width and text size and is a parameter of a text (command `info`):

$$ratio = \frac{\text{line width} * 100\ \%}{\text{text size}} \quad (2)$$

Here an example: If the line must be of a width of minimal 0,125mm and the text itself is 1mm in size, the required ratio equals to:

$$12{,}5\ \% = \frac{0{,}125\ mm * 100\ \%}{1\ mm}$$

CAUTION: *EAGLE* DRC does NOT perform a line width check for structures in non-copper layers !

In other words: **The silk screen line width is not checked by DRC.**

Most frequently the text holding the name of the part (in layer tNames/bNames) has to be adjusted regarding its position, orientation, size and of course ratio. By default the name is hard locked to the origin of the part. Using the command `smash` this fixed connection gets broken. So I recommend following steps for the top side of the board:

- display only layer Dimension(20), tPlace (21), tOrigin (23), tNames(25) and tStop (29)
- group all objects or run command `group all`
- smash group or run command `smash;`
- rearrange the names, adjust size and ratio (commands `move` , `group` and `change`).

Proceed with the bottom side if required:

- display only layer Dimension(20), bPlace (22), bOrigin (24), bNames(26) and bStop (30)
- group all objects or run command `group all`
- smash group or run command `smash;`
- rearrange the names, adjust size and ratio (commands `move` , `group` and `change`).

CAUTION: Equation 2 on page 47 implies that the smaller the text gets, the more ratio is required for the affected text.

If you need to verify the minimal line width of all names, there is a workaround to force the DRC checking it at the top side of the board. Please backup your project files before proceeding with the following steps:

1. Start the DRC, change into section “Layers” and invent a dummy layer as shown in Figure 36. The layer number, in our case #7 - does not matter. The layer **must not** contain any object. Even if your board is multilayer, just create another layer. The number real usable layers with this workaround is limited to 15. Of course your license must allow this step.

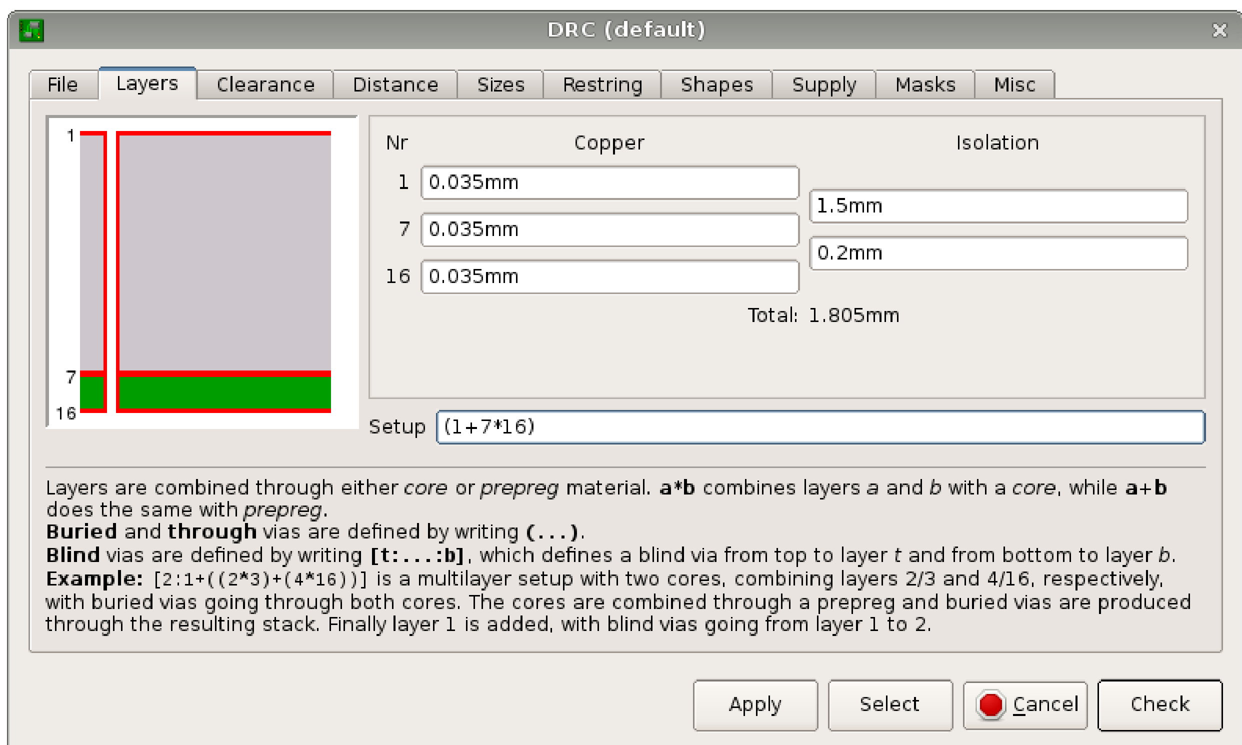


Figure 36: DRC Dummy Layer

2. Change into section “sizes” and enter the minimum line width as shown in Figure 37.

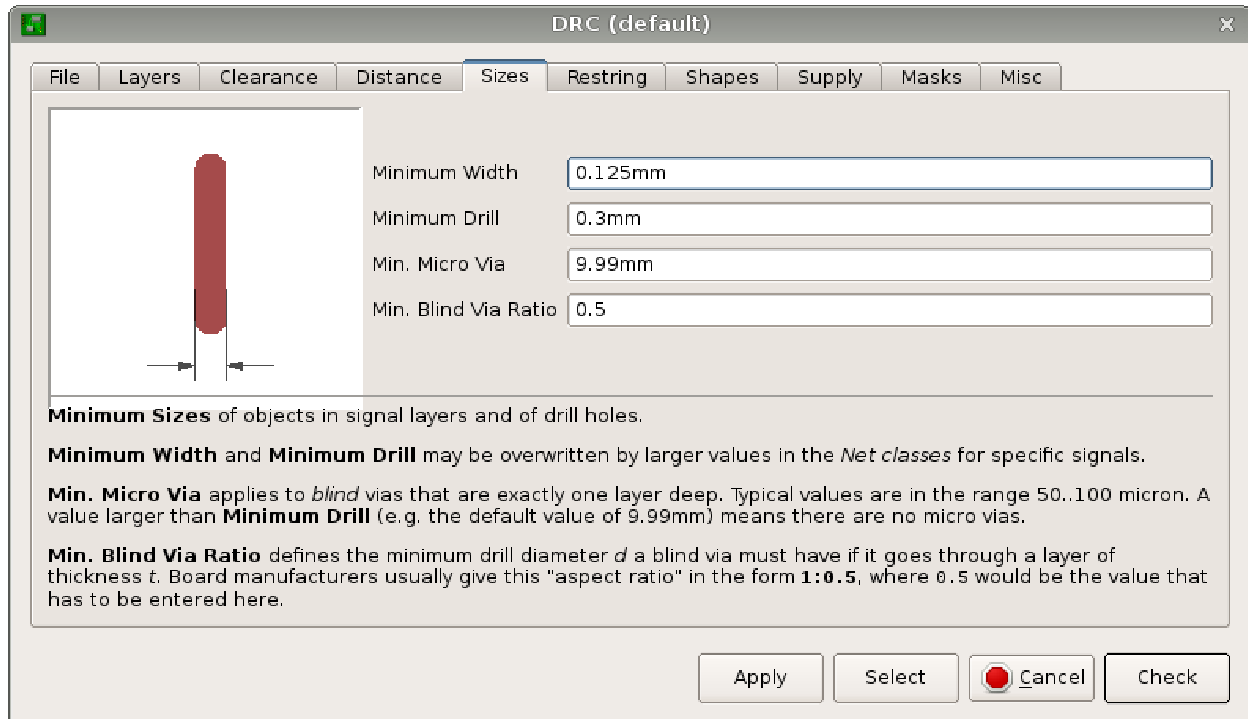


Figure 37: DRC dummy layer sizes

3. click “Apply” and close the DRC window.[13]
4. display only layer tNames(25)
5. group all objects or run command `group all`
6. Transpose the group into your dummy layer (command `change`). By the color change the result is easy to see.
7. Now run DRC again. Now that the names of the parts are in a copper layer, the DRC checks for a minimal line width of 0,125mm - in my example here. See Figure 38. The DRC may output lots of overlap-errors which result from the texts overlapping with inner-layer vias and pads. Just ignore these errors and look for width-errors, for they belong to texts drawn with a ratio too small to meet your constraints.
8. After you have ironed out the width-errors, re-run DRC to make sure everything is fine. Then group all objects again.
9. Transpose the group back into layer tNames (25) and you are done.
10. Optional: Perform the DRC check as described in section 6.2.4.1 page 45.

13 These dummy settings can be saved in a special dru file in section “File”.

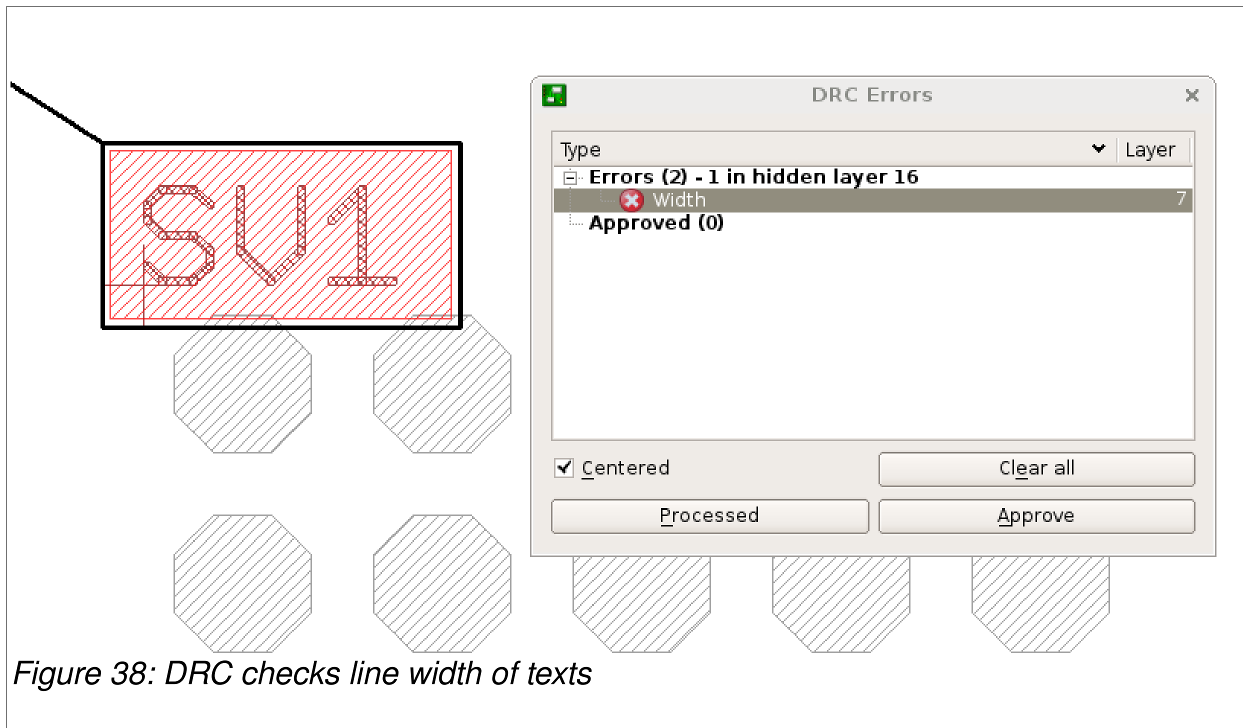


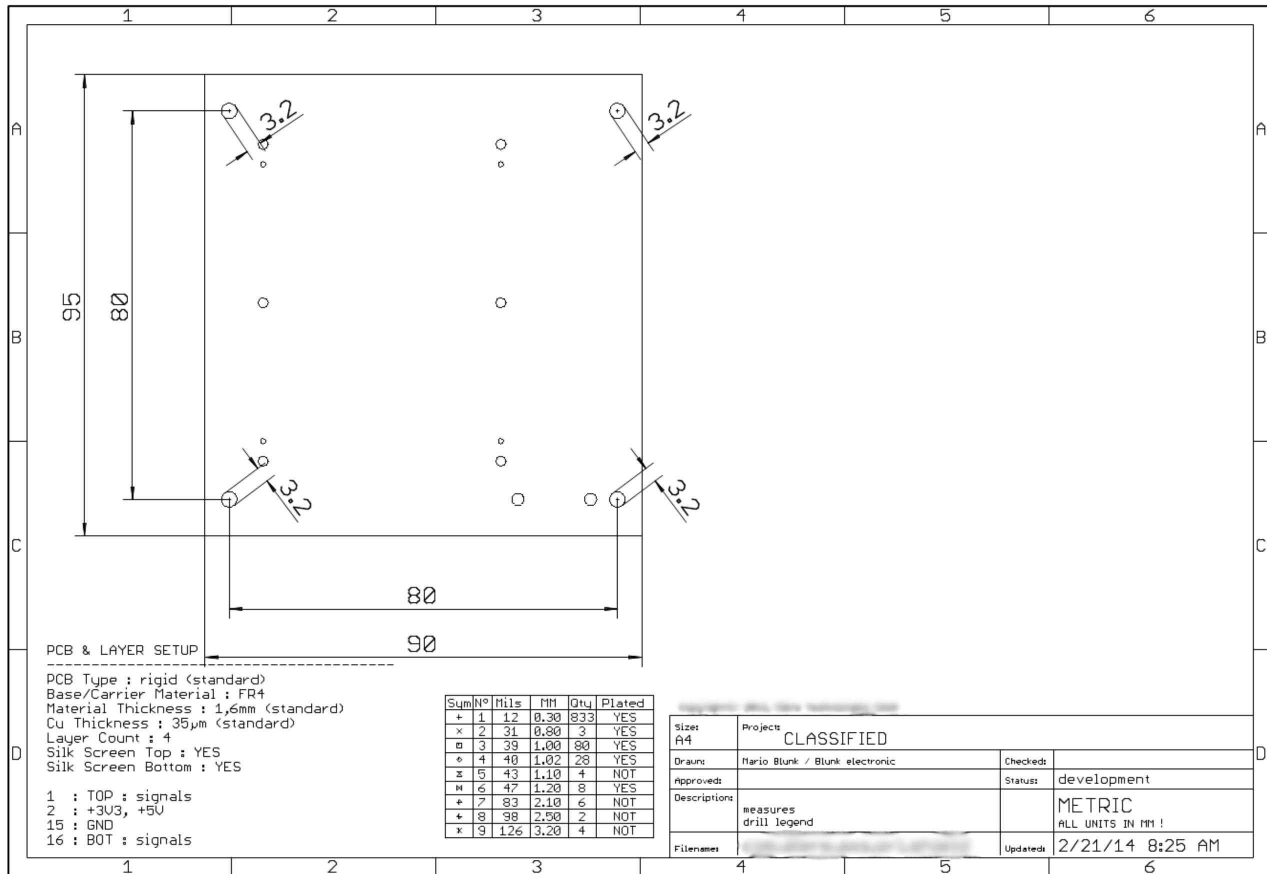
Figure 38: DRC checks line width of texts

Repeat these steps for the bottom side of the board if necessary.

7 Generating CAM Files

7.1 PCB specification

1. Make sure the PCB specification is written in both: a reserved gerber file dedicated for documentation only and/or in a dedicated pdf file. See example in Figure 39.



Sym	N°	Mils	MM	Qty	Plated
+	1	12	0.30	833	YES
×	2	31	0.80	3	YES
	3	39	1.00	80	YES
	4	40	1.02	28	YES
	5	43	1.10	4	NOT
	6	47	1.20	8	YES
	7	83	2.10	6	NOT
	8	98	2.50	2	NOT
	9	126	3.20	4	NOT

Figure 39: PCB specification

7.2 Placement Coordinates

1. Make sure the partlist gets exported from a board (see Text 1 page 7) !
2. Alternatively use the ulp `mountsmd`.

7.3 Design Rules

1. Run the DRC with the design rules provided by the PCB manufacturer **before** generating CAM files.

7.4 CAM Processor

Numerous parameters are to be cared for when setting the CAM processor. Check if:

1. extended Gerber format RS-274X is applied
2. proper drill data format is set (i.e. Excellon)
3. correct layers get exported into the respective gerber file
4. plated and non-plated drills are output in separate drill data files
5. plated millings are output in a separate gerber file
6. mirroring of layers matters (default: no mirroring)
7. CAM files legend is provided for PCB manufacturer

7.5 Bill of Material (BOM)

1. If attributes are used to hold particular part codes of components, make sure they match package and value of the device affected.

   Example: There is an SMD 0805 resistor R101 with value 100Ohms. The attribute PART_CODE_xyz must be R_PAC_S_0805_VAL_100. The suitable EAGLE command to edit attributes is ATT. (See Figure 6 page 12).

   The PART_CODE_xyz attribute affects the BOM created later.

   Wrong attributes lead to wrong material lists and wrong device fittings !

WARNING :

ATTRIBUTES ARE USER SPECIFIC ENTRIES. EAGLE DOES NOT VERIFY THEIR CORRECTNES !

2. Verify the part code complies with corporate conventions. Read more in (8).

8 Appendix

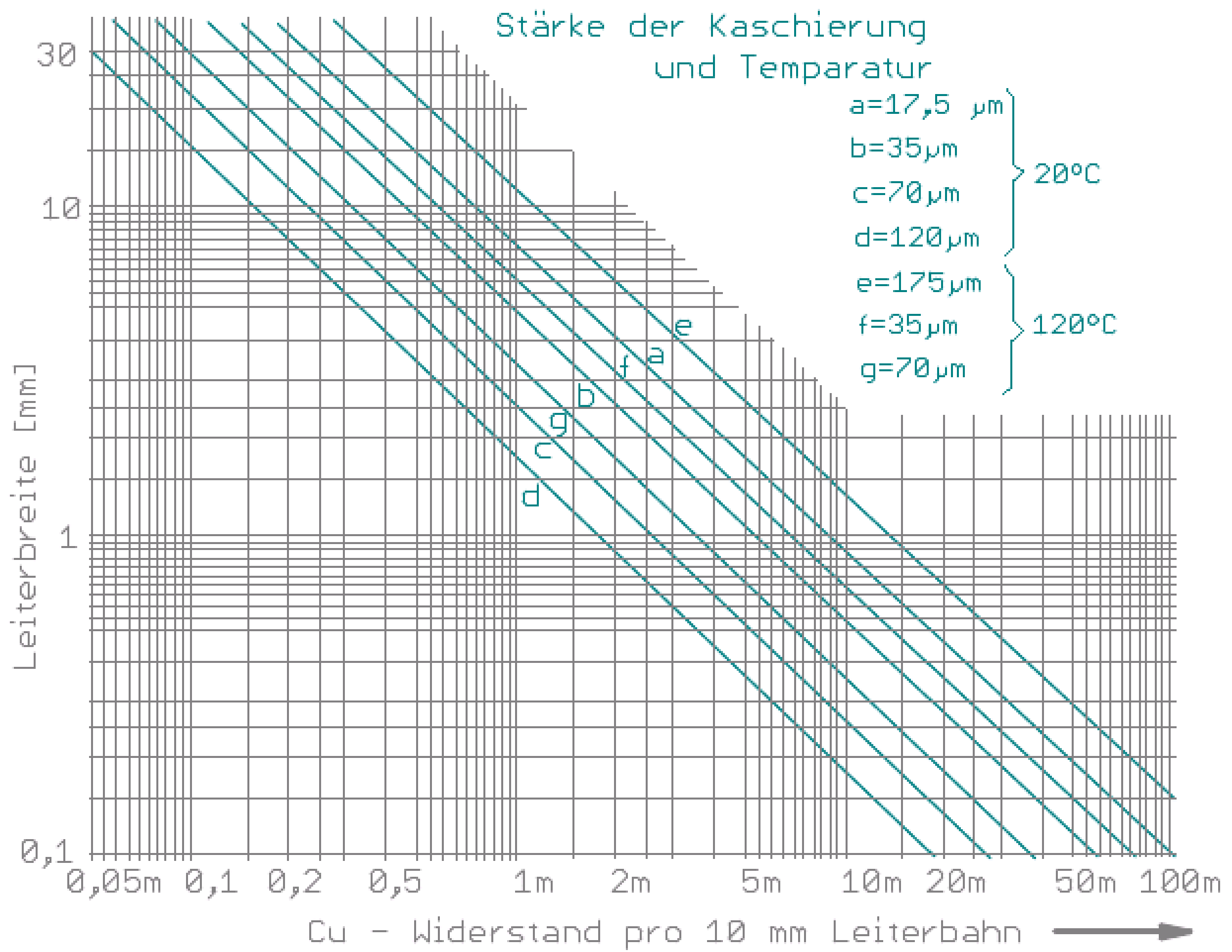


Diagram 1: maximum current load vs track width at various temperatures

German	***English***
Stärke der Kaschierung und Temperatur	thickness of copper coating and temperature
Leiterbahnbreite	track or wire[14] width
Widerstand pro 10mm Leiterbahn	resistance per 10mm track/wire length

14 The EAGLE terminology uses the word “wire” for all kinds of lines regardless if this is real copper or just documentation or measurement.

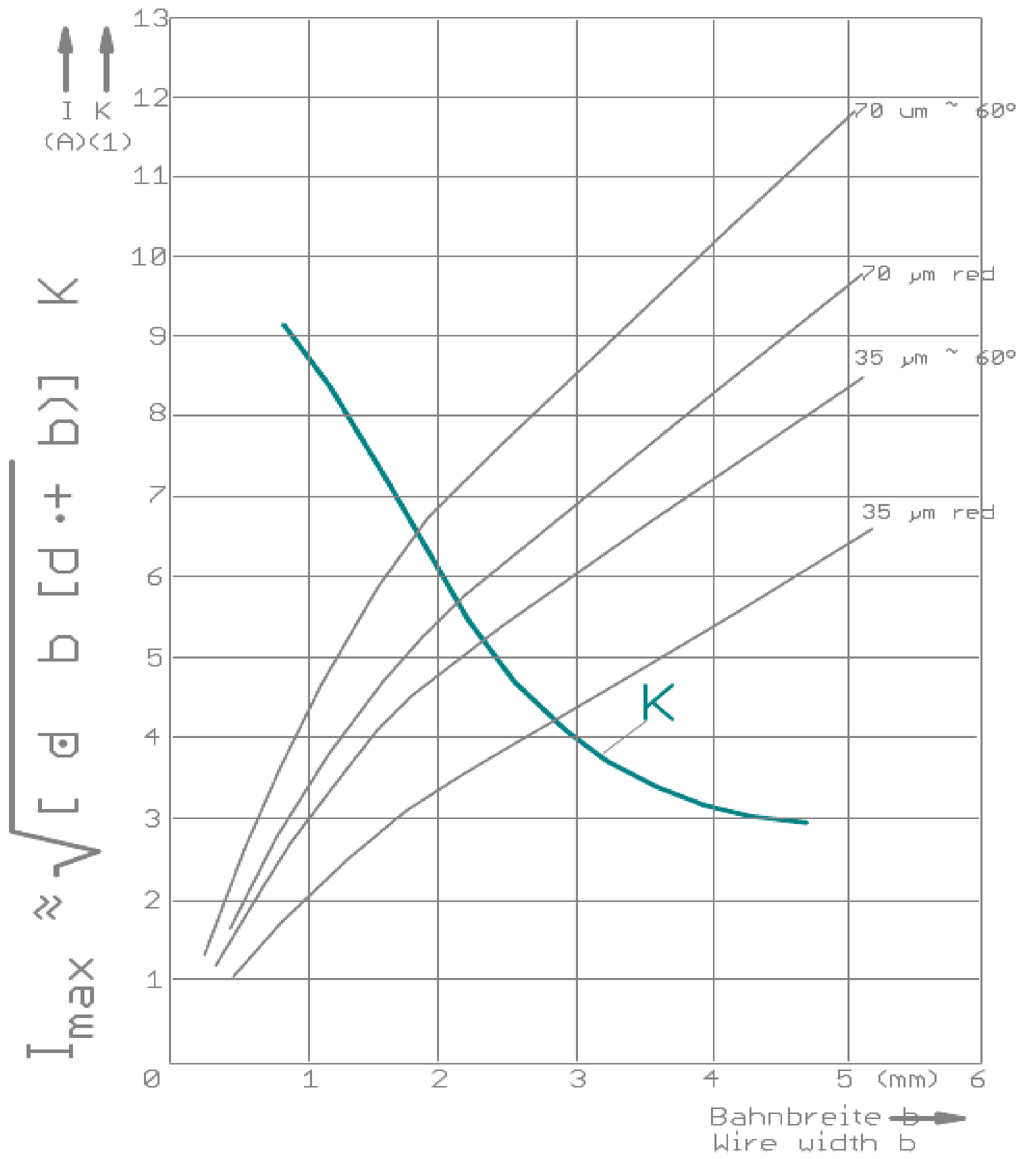


Diagram 2: maximum current load vs track width at various temperatures

Metall	spez. Widerstand bei 20 °C ρ $\left[\frac{\Omega \cdot mm^2}{m}\right]$	Temperaturbeiwert α $[10^{-3} / °C]$
Kupfer	0,0174	4,33
Silber	0,0159	4,10
Gold	0,0224	4,0
Nickel	0,078	6,75
Zinn	0,123	4,6
Blei	0,208	3,8
Palladium	0,108	3,77
Rhodium	0,0454	4,43

Leiterbahnwiderstand

$$R = \frac{\rho \cdot l}{d \cdot b}$$

l [mm] = Länge der Leiterbahn

d [µm] = Stärke der Kaschierung

b [mm] = Breite der Leiterbahn

R [Ω] = Leiterbahnwiderstand

Beispiel :

Leiterbahnlänge l = 50 mm

Kupferkaschierung d = 35 µm

Breite b = 1 mm

$$R = \frac{\rho \cdot l}{d \cdot b} = \frac{0{,}0174 \cdot 50}{35 \cdot 1} = 24{,}9m\ \Omega$$

Table 1: track/wire resistance calculation of various conducting metals

German	***English***
spez. Widerstand bei	specific resistance at
Temperaturbeiwert	temperature coefficient
Leiterbahnwiderstand	resistance of track/wire
Länge der Leiterbahn / Leiterbahnlänge	length of track/wire
Stärke der Kaschierung / Kupferkaschierung	thickness of coating / copper thickness
Breite der Leiterbahn	track/wire width
Kupfer (Cu)	copper
Silber (Ag)	silver
Zinn (Sn)	tin
Blei (Pb)	lead
Beispiel	example
Breite	width

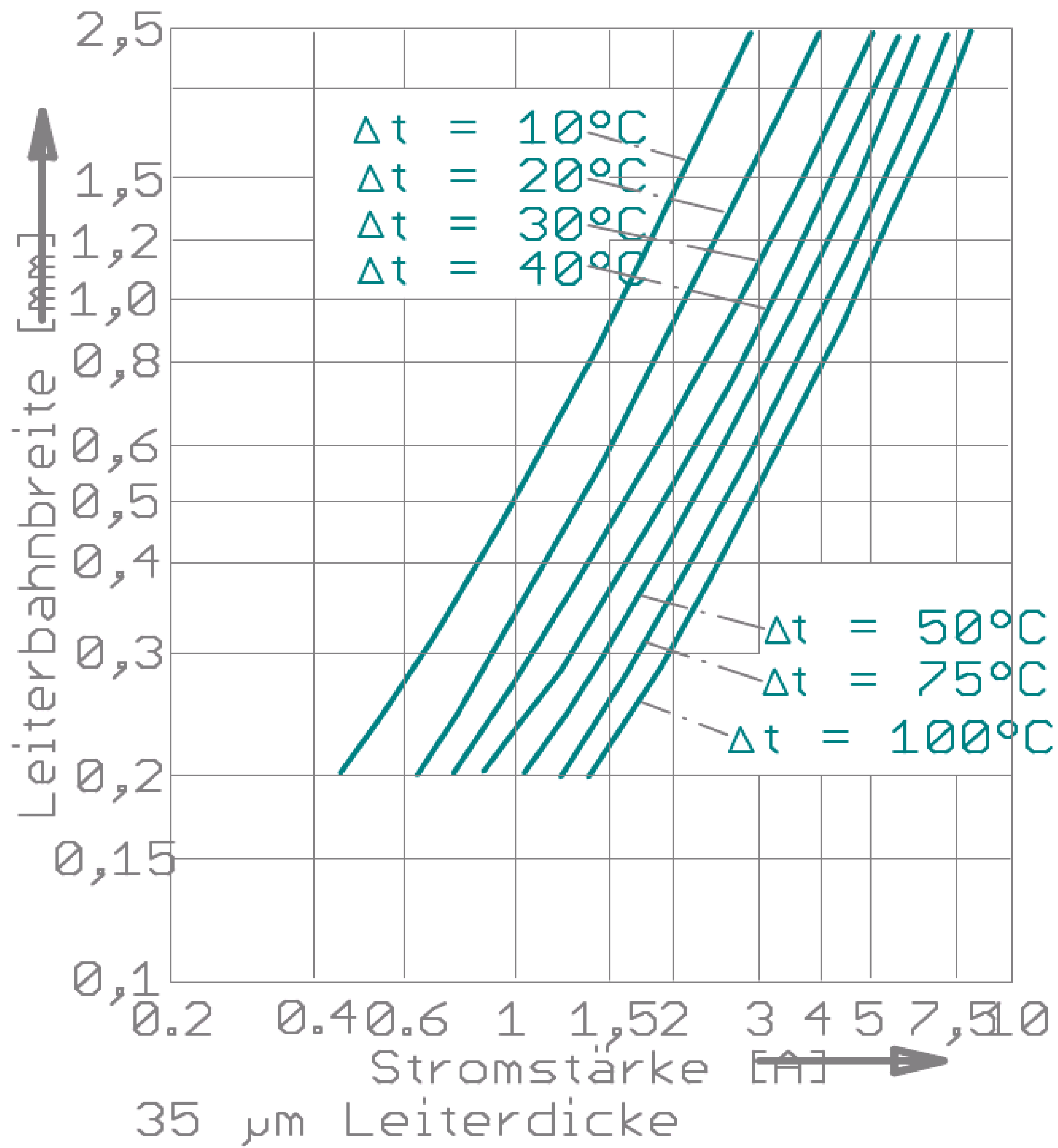


Diagram 3: maximum current load vs track width at various temperatures

German	***English***
Leiterbahnbreite	track/wire width
Stromstärke	(electrical) current
Leiterdicke	track/wire thickness

Isolationsabstand von Leiterbahnen (USA MIL-Std. 275B)

A = normale Umweltbedingung
B = staubige/schmutzige Umgebung
Spannungswerte für Gleichspannung bzw. Spitzenwert der Wechselspannung

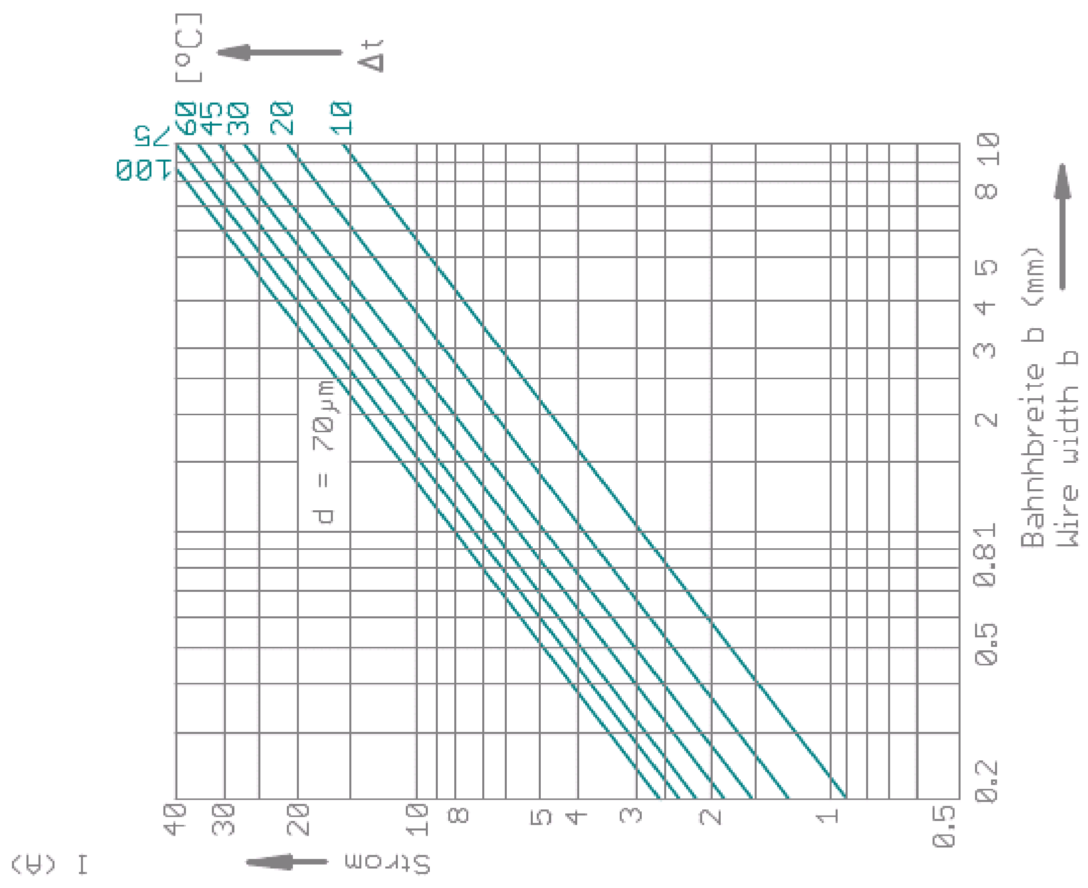
Spalte I   ohne Schutzüberzug in Höhen von 0 ... 3048 m
Spalte II ohne Schutzüberzug in Höhen über 3048 m
Spalte III mit Schutzüberzug in Höhen von 0 ... 3048 m
Spalte IV mit Schutzüberzug in Höhen über 3048 m

Spannung [V]	IA	IB	II	III	IV
0 ... 50	0,381	2,032	0,660	0,381	0,559
51 ... 100			1,575		0,762
51 ... 150	0,660	2,032		0,559	
101 ... 170			3,17		1,524
151 ... 300	0,575	3,17		0,762	
171 ... 250			6,35		3,17
301 ... 500	3,17	6,62		1,524	
251 ... 500			12,70		6,35
> 500	0,0076 a Volt	0,0152 a Volt	0,025 a Volt	0,0051 a Volt	0,0127 a Volt

Die angegebenen Zahlen sind Mindestwerte in mm.

Table 2: clearances between tracks/wires

German	***English***
Isolationsabstand von Leiterbahnen	clearance between tracks/wires
normale / staubige / schmutzige Umweltbedingung	normal / dusty / dirty environment
Spannungswerte für Gleichspannung bzw. Spitzenwert der Wechselspannung	DC voltage or AC peak voltage
Spalte	column
ohne/mit Schutzüberzug in Höhen von/über x m	with/without protective coating at altitudes of/above x **Meters**
Spannung	voltage
Die angegebenen Zahlen sind Mindeswerte in mm.	Numbers given are minimal values in **Millimeters**.



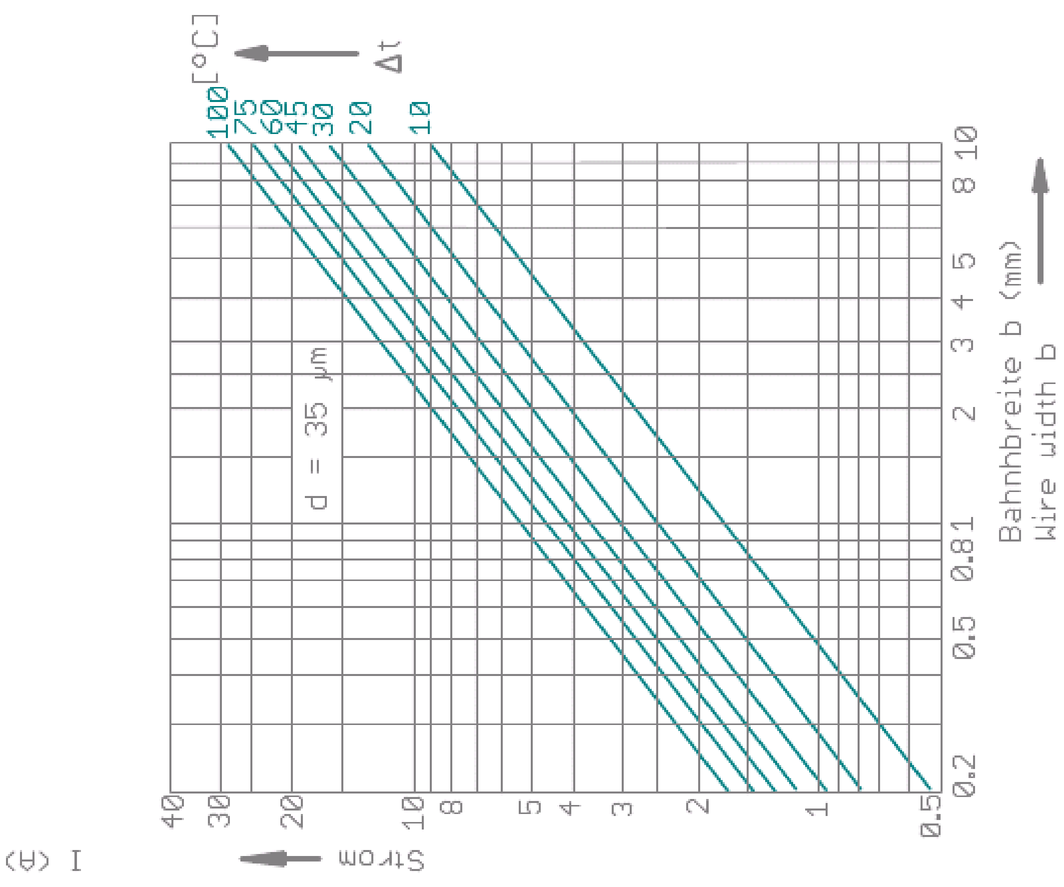


Diagram 4: maximum current load vs track width at various temperatures

9 Useful Links

(1) *CadSoft EAGLE Consulting* – a reasonable way to reasonable work at http://www.blunk-electronic.de

(2) An *EAGLE* configuration script eagle.scr . Units, grid, line with, text size, font, drills and more – well defined and cleaned up ...

(3) Find updates of this checklist at http://www.blunk-electronic.de/cad.html

(4) What is Boundary Scan ?

(5) Looking for a lean **Boundary Scan Test System** ? Please have a look **here !**

JTAG/Boundary Scan
System M-1
according to Std. IEEE 1149.1

- Minimal UUT access via 5 wire IEEE1149.1 test bus
- Fault diagnosis down to pin level
- Interconnect Test (short/open detection)
- Memory-Connect Test (RAM/ROM/FLASH)
- Oscillator Test / Clock Test
- LED, Display Test, Logic Test ...

- UUT Power Switch and Monitoring up to 6A / 48 V DC
- full galvanic separation of UUT from Scan Master in Non-Test Mode
- Operator Activity reduced to pushing START / STOP Button
- PASS / FAIL display by just two front panel LEDs

Contact: Mario Blunk / Blunk electronic / Buchfinkenweg 5 / 99097 Erfurt / Germany
info@blunk-electronic.de www.train-z.de Phone +49 361 518 9618 / +49 176 290 45 855

(6) Debug SPI, I²C, Boundary Scan/JTAG and other hardware with the *Logic Scanner* at http://www.blunk-electronic.de/logic_scanner/Logic_Scanner_UM.pdf

(7) *EAGLE* - an affordable and very efficient schematics and layout tool at http://www.cadsoftusa.com

(8) A Gerber Data Viewer and Editor at http://www.pentalogix.com

German Sales and Support Office:

Helmut Mendritzki
Software-Beratung-Vertrieb
Dahlienhof 1
25462 RELLINGEN
GERMANY
Tel.: +49 (0) 4101 - 20 60 51
Fax: +49 (0) 4101 - 20 60 53

Mobile: +49 (0) 171 - 2155852
eMail: mendritzki@aol.com

(9) The office alternative : *LibreOffice* at http://www.libreoffice.org

10 References

(1) Mario Blunk, "*EAGLE Library Tutorial"* at

http://www.blunk-electronic.de/pdf/library_tutorial.pdf

(2) Joachim Franz "*EMV Störungssicherer Aufbau elektronischer Schaltungen*" ; German; ISBN 978-3-8348-0893-6

(3) *CadSoft EAGLE* Version 6.x English users manual

(4) Stencil Desgin Guidelines IPC-7525A, February 2007

(5) Hans-Joachim Fischer / Wolfgang E. Schlegel, "*Transistor- und Schaltkreistechnik*" ; PP313-326 ; German; ISBN 3-327-00362-9

(6) The Institute of Electrical and Electronics Engineers, Inc. , 3 Park Avenue, New York, NY 10016-5997, USA; IEEE Std 1149.1-2001 "*IEEE Standard Test Access Port and Boundary-Scan Architecture*"

(7) Mario Blunk, "*A Guide to test methods and why to go for Boundary Scan*" at http://www.blunk-electronic.de/bsm/how_to_test.pdf

(8) Mario Blunk, "*Conventions on Naming and Displaying Objects in CadSoft EAGLE drawings*"

(9) Mario Blunk, "*Equalizing Brightness of Standard LEDs*" at

http://www.blunk-electronic.de/pdf/LED_brightness_adjustment.pdf

(10) Mark I. Montrose, "*Printed Circuit Board Design Techniques for EMC Compliance*", A Handbook for Designers" ; IEEE Press Series on Electronics Technology

11 Disclaimer

This document is believed to be accurate and reliable. I do not assume responsibility for any errors which may appear in this document. I reserve the right to change it at any time without notice, and do not make any commitment to update the information contained herein.

Blunk electronic / Buchfinkenweg 3 / 99097 Erfurt / Germany / Tel. +49 176 2904 5855 / www.blunk-electronic.de

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