Selection Guide on how to test Boards and Systems

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Abstract: *Guideline to decide the proper test method for boards and systems in an assembly line of an EMS provider or in the field. Questions relevant for the operator as well as the test engineer who decides about the deployment of Boundary-Scan test equipment. Specials regarding the benefits of Boundary-Scan acc. to IEEE 1149.1 are also touched.*

Keywords: *Boundary-Scan, JTAG, IEEE1149.1, nets, DFT, SMD, THT, FPGA, CPLD, CPU, MCU, pull resistors, prototype, soldering, reflow, shorts, stuck-at, connectors, I²C, functional test, in-circuit-test, flying-probe-test, test run time, operator, nail, price, financial investment, integration, setup time, complexity, lean*

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1 Introduction

This document aims to provide a guide to select an appropriate test method according to the actual board or system – further-on referred to as UUT (Unit Under Test) – to be tested. An overview of test methods with their individual pros and contras will be given in an impartial manner.

I appreciate all critics to improve the quality of this document !

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2 Test Methods of the Art

2.1 Functional Test (FT)

The easiest way to test an assembled UUT is the functional test (FT): Connect the UUT with all connections required, power-up and see what happens. Obviously this method only tells you about GO or NOGO. A detailed report of faults is close to impossible to get unless the operator has gained a lot of experience over dozens of test runs.

WARNING: The idea for FT might give the impression of an easy to get test at lowest price. Depending on the complexity of the UUT this assumption may prove true or may lead into endless attempts to repair boards, thus raising unacceptable costs.

FT in general always happens on system level. System test – several boards connected to each other e.g. in a rack – is possible, but the test result comes also on system level ! FT never outputs something like “Net ADR4 is stuck at low.” Instead the whole UUT does not work or fails partially which in turn raises questions and speculations about the actual fault. Imagine a CPU with some memory IC around. If only one of let say 32 address and 16 data nets is broken, the whole UUT will not come to life. Good luck finding the fault by functional testing...

WARNING: As the complexity of the UUT increases, FT covers less possible faults. The test run time required to go through every combination of states increases exponentially. In order to save time, lots of combinations will not be tested for sure ! So the result PASS of a complex UUT test is more of psychological nature.

Functional Test is a high-level system test to locate faults in a late production state of the UUT !

This statement implies: If a fault is detected while FT, a lot of labor has been invested into the UUT already e.g. wires soldered, housing assembled, series numbers noted, … . All those steps have to be repeated all over again until the board passes the FT !

A very simple UUT can be tested with FT. Very simple means: A fault can be located with reasonable and acceptable efforts as time and material goes.

Table 1 gives an overview of pros and contras of FT.

PRO	CONS	REMARKS
low price test equipment		- if UUT is very simple
space requirements		- app. 1m²
short setup time		
simple test equipment		
time to adapt modifications		
test run time		- depends on how many functions and states are to be tested (see discussion above)
	fault detection in a very late production state	
system test		
	Faults may pass the test undetected. → **UUT fails at the customer site**	
	poor fault diagnosis → **increased labor costs**	
	high skilled personal required for test operation	- if complex functions are to be tested
	error prone tasks while test operation	- if complex functions are to be tested
no serious preparation for testing required		- so called Design For Test (DFT)

Table 1: Pro and Contras of Functional Test (FT)

2.2 In-Circuit-test (ICT)

A powerful workhorse of board test over decades has been and still is the In-Circuit-Test (ICT). It allows a low level board test for the majority of boards assembled around the planet with a very detailed fault report.

As the boards are getting more dense in regard to the number of layers, the via types (buried and blind vias), pin spacing, pin accessibility (BGAs) the ICT is loosing ground. ICT-Nails can't be placed everywhere and a certain clearance between them must be guarantied. The more nails, the greater the force required to push the adaptor onto the board. Every test pad and every nail poses an extra capacitive and inductive load onto the affected net, and not to forget: eventually there is no more space left to place test pads or test points in the PCB layout.

In-Circuit-Test implies a financial burden of several thousands of Euro or Dollar for the nail adaptor to be manufactured, not to mention the ICT machine itself. As soon as the affected board undergoes modification or is discontinued, a very expensive piece of scrap moves into a dusty shelf. Concluding, the price is the major drawback of ICT.

In-Circuit-Test is a low-level structural test to locate faults in an early production state.

Table 2 gives an overview of pros and contras of ICT.

PRO	CONS	REMARKS
	high price test equipment	
	long setup time	- concerning making the nail adaptor and wiring underneath
	space requirements	- min. $2m^2$
	complex and high skilled test equipment	
	time to adapt modifications	- In best case dismantling the adaptor, modifying nails, changing wiring required. - In worst case the whole nail adaptor has to be made anew. - Software changes are negligible.
test run time		- usually a matter of seconds
fault detection in an early production state		
	no reuse of test equipment	- concerning the nail adaptor and wiring underneath
mixed signal test		
	extra space required at the UUT	- for test points or test pads
	extra capacitive or inductive load on the UUT signals	- non-test-mode and performance may be negatively affected
	system test not possible	
Close to all faults get detected.		- provided there are sufficient test points
Very good fault diagnosis → **minimal labor costs**		
low skilled personal required in test operation		
error safe tasks while test operation		
	careful preparation for testing required	- so called Design For Test (DFT)

Table 2: Pro and Contras of In-Circuit-Test (ICT)

2.3 Flying-Probe-Test (FPT)

A wonderful example of human ingenuity is the Flying-Probe-Test (FPT) – an “adaptable ICT” with so called “flying nails” which can contact the board at every exposed copper area like SMD-pads, THT-pads, vias, test pads, … Such a machine outnumbers the price of a home (200T – 500T EUR). So most EMS providers can't afford it.

Flying-Probe-Test is a low-level structural test to locate faults in an early production state.

PRO	CONS	REMARKS
	very high price test equipment	
short setup time		
	space requirements	- min. 3m²
	complex and high skilled test equipment	
time to adapt modifications		
	test run time	- depends on number of test points and board size
fault detection in an early production state		
reuse of test equipment		
mixed signal test		
	system test not possible	
Close to all faults get detected.		
Very good fault diagnosis → **minimal labor costs**		
low skilled personal required in test operation		
error safe tasks while test operation		
no serious preparation for testing required		- so called Design For Test (DFT) - if nails are to contact device pads and pins

Table 3: Pro and Contras of Flying-Probe-Test (FPT)

2.4 Boundary Scan (BST)

Initiated by the problem of limited space for test points, the growing density of parts fitted, the inaccessibility of nets (multilayer PCBs combined with BGA packages) the standard IEEE1149.1 has been ratified in the early nineties. Bulky test pads or test points have moved inside the integrated circuits (ICs). The access to those points is now adaptor-less, thus dramatically reducing the financial investment and increasing the flexibility to adapt UUT modifications.

IEEE1149.1 is entirely made for digital board tests. Mixed signal test can be achieved with lots of restrictions. Analog signal testing is not possible. There is the IEEE1149.4 standard for mixed signal test but it never made it into real life, unfortunately. Further on there is IEEE1149.5 (system test, but was discarded eventually), IEEE1149.6 (AC coupled digital test) and IEEE1149.7 (extension of IEEE1149.1 with an advanced bottom hardware layer).

However, IEEE1149.1 is the workhorse of boundary scan, frequently referred to as JTAG, which is a dutch company, based in Eindhoven, that provides boundary scan test systems.

WARNING: It should be noted that the Boundary-Scan-Test is no *Wunderwaffe* as advertised in some publications. As mentioned in Table 4 below, the UUT itself must have fitted at least one IC fully supporting IEEE1149.1. *The IC implies testability !*

In contrast to the early beginnings of IEEE1149.1 in the nineties, today the majority of CPLDs, FPGAs, CPUs, DSPs and Microcontrollers (MCUs) supports the standard by default. Presently the majority of boards used in the sector of telecommunication, entertainment, networking, industrial control, medical, avionics, military and automotive bear ICs that do support IEEE1149.1.

Boundary-Scan-Test is a low-level structural test to locate faults in an early production state.

The fact that the UUT has to be powered up during BST can be regarded both as curse and as blessing at the same time. A fully powered up UUT with unlucky paced faults tends to self-destruct unless careful power monitoring is done. But, the advantage of a powered up UUT and low-level access to pins allows testing of peripherals like displays, LEDs, relays, motor drivers in a production stage where no firmware etc. has been programmed into the UUT yet !!! With some programming efforts, system test is possible !

It is obvious that entirely analog designs like an audio-amplifier are excluded from Boundary-Scan-Testing. BST is also oversized for testing a board with a simple monoflop-driven relay stage ...

The first and most crucial point in Table 4 addresses the financial investment in a BST-System. Usually small or start-up companies can't afford to by it. As a result of this shortage they either do not take orders to

manufacture BST-capable boards or they default to functional test (FT) or optical inspection. An extra load is imposed by add-ons like maintenance contracts and thereof.

Table 4 gives an overview of pros and contras of BST.

PRO	**CONS**	**REMARKS**
	very high price test equipment	- if the test system is closed source 20T – 50T EUR (plus extra price for maintenance and support),
short setup time		- from a few hours to one week, depending on UUT complexity
	space requirements	- min. 0.5m²
	complex and high skilled test equipment	
time to adapt modifications		- a matter of minutes
test run time		- from a few seconds to 10 minutes (depending on the UUT complexity)[1]
	UUT powered up is mandatory	- power monitoring required
fault detection in an early production state		
reuse of test equipment		
	mixed signal test	- very restricted possible with IEEE1149.1
system test possible		- several boards connected to each other e.g. in a rack
Close to all faults of digital nets get detected.		- provided the fitted ICs support IEEE1149.1
Very good fault diagnosis → **minimal labor costs**		- provided the fitted ICs support IEEE1149.1
low skilled personal required in test operation		
error safe tasks while test operation		
	integration into other test systems	- provided the UUT can be galvanically separated from all test systems

1 These figures apply for the test procedure only. If additional data is to transferred into the UUT e.g. In-System-Programming (ISP), the time required is significantly more (in worst case up to 1hour).

	careful preparation for testing required	- so called Design For Test (DFT)

Table 4: Pro and Contras of Boundary-Scan-Test (BST)

3 References

- The Institute of Electrical and Electronics Engineers, Inc. , 3 Park Avenue, New York, NY 10016-5997, USA; IEEE Std 1149.1-2001 "*IEEE Standard Test Access Port and Boundary-Scan Architecture*"

4 Disclaimer

This document is believed to be accurate and reliable. I do not assume responsibility for inaccuracies any errors which may appear in this document. I reserve the right to change it at any time without notice, and do not make any commitment to update the information contained herein.

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